IBM SCHOOL COMPUTER PROJECT

IBM *IBM Australia Limited* (*Incorporated in New South Wales*)

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November 8, 1972.

The Principal,
Caringbah High School,
Willarong Road,
CARINGBAH. N.S.W. 2229

Dear Sir,

Confirming arrangements made at our last progress meeting, the Mini Computer Project will conclude on Friday December 1, 1972.

I would appreciate it if your computer could be delivered to our Office at Lidcombe on the morning of Friday, December 8 for judging. The judges are Mr. J. Willis, Director, Museum of Applied Arts & Sciences, Mr. D. Williamson and Mr. J. Griffiths, Senior Instructors, IBM Customer Education.

Please do not worry if it is not completed as the judges would like to see how far you have progressed. Naturally, the completed job is the one which will attract the most points - but, how many have completed the job?

Two copies of the written report should accompany the computer. For your guidance, the attached outlines the information the judges will be seeking in the report.

Presentation of Cheques will take place on Wednesday, December 6 at The Museum of Applied Arts & Sciences, Harris Street, Ultimo, to which you are all invited. Please let me know who will be attending.

The computers will be on display at the Museum and returned to each school by arrangement.

...2/

IBM

I would like to express my appreciation for the interest shown by your school in this project. I trust the students have gained a greater insight into the mysteries of computers and that they will continue this interest throughout their student days.

Yours sincerely,
IBM Australia Limited,

R.C. Ctercteko,
Contributions Program Manager.

RC:eh:172

CC Mr. P. Jones,

IBM

SCHOOL COMPUTER PROJECT

CONSTRUCTION COMPETITION

In December, 1972 a prize will be awarded to the school whose computer project is judged to be the best by the judges Mr. D.A. Williamson and Mr. J.M. Griffiths, Instructors of IBM and Mr. J. Willis, Director of Museum of Applied Arts and Sciences.

The following points will be considered in deciding the winner:-

1. Construction -

    (a) Quality of Finish and Appearance.

    (b) Internal layout, mechanical and electrical.

    (c) Performance.

2. A paper prepared by the students involved detailing the following points and being between 600 and 1000 words long.

    (a) The number and forms of the students directly involved.

    (b) The history of the project at their school.

    (c) Any significant things learnt of difficulties encountered during project.

IBM "CONTACT" ENGINEERS

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649.0133 ext. 556	Mr. D. Williamson	Sydney Teachers' College William Balmain College
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929.0688	Mr. A. Malikoff	Sydney Church of England Grammar School North Sydney Boys' High School

The above Engineers are available to assist you by guidance should you have any problems.

Please endeavour to solve the difficulties yourselves before contacting your "counsellor".

If he is not available, then you may contact any of the above.

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SCHOOL COMPUTER PROJECT

MANUAL PREPARED BY: D.A. Williamson, Senior Instructor, IBM Customer Engineering
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PROMOTED BY: IBM Education Relations Program

SIGNED ASSYNCHRONOUS BINARY ADDER

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SIGNED ASSYNCHRONOUS BINARY ADDER

CHAPTER 1

NUMBERING SYSTEMS AND LOGIC

CHAPTER 1.

NUMBERING SYSTEMS AND LOGIC

General

There are several types of numbering systems in use to-day throughout the world. However, the most common system is the decimal system. Since it is necessary to have a good understanding of the numbering systems which are used in digital computers, it is necessary to study several basic systems. The most common numbering system used in computer logic is that of binary. Quite often, the binary system is modified to what is commonly called BCD or the binary coded decimal system. In the SABA unit a binary numbering system is used. In addition, it may be helpful to use another numbering system to assist in the conversion from decimal to binary or from binary to decimal. This system is called the octal system and is sometimes referred to as the shorthand code for the binary system.

In order to understand the binary and octal systems clearly, it is necessary to first review the basic fundamentals of all numbering systems and particularly the decimal system, with which we are most familiar.

Decimal System

A number system is a method of counting. Various number systems differ only in the number of symbols that are used for counting. The familiar decimal system has ten symbols, which may be combined to represent any decimal number. The base of the decimal system is ten, because it has ten symbols, 'zero', which normally represents the quantity 'none', and one through nine.

When starting the count of 'one' in the decimal system, and counting in sequence, the count can bontinue up to 'nine' without running out of symbols. Therefore, to count higher than nine, a method must be devised to make use of some combination of these ten symbols. The simplest of such combinations involves two symbols, or digits, so arranged that the symbol on the left (ten's digit) tells how many times the count has run out of symbols - that is, how many 'ten's' there are - and the symbol on the right (unit's digit) tells how many items counted since last passing

a whole multiple of ten. Thus, $23=2 \times 10 + 3$. Ten symbols were used twice, and then three more were added. Another way of stating this, is that the number 23 represents two '10's' and three '1's'. The decimal system is further extended to include the hundred's digit, thousand's digit, etc.

Examine a counter with the number | 9 5 8 3 | in it.

The symbol in the right hand position, three, shows that of the total quantity counted, there are three units or '1's' while the symbol immediately to the left of the unit's position indicates there are eight '10's', the five represents five hundreds, and the nine represents nine thousands. Thus, $9,583 = 9,000 + 500 + 80 + 3$. This shows that the decimal system provides a means of representing numbers that can be expressed by a sum of terms. Each individual term consists of a product of a power of ten and a digit from zero through nine. For example, the number 9,583 can also be written in the following manner:

$$(9 \times 10^3) + (5 \times 10^2) + (8 \times 10^1) + (3 \times 10^0)$$

The multipliers in the above example such as 10^3, 10^2, and 10^1, and 10^0 are equal in value in the decimal system to the following:

$$10^0 = 1,\ 10^1 = 10,\ 10^2 = 100, \text{ and } 10^3 = 1,000.$$

The exponent or the power to which ten is raised, is equal to the number of zero's to the right of one.

$$\begin{aligned} 1 &= 10^0 \\ 10 &= 10^1 \\ 100 &= 10^2 \end{aligned} \qquad \begin{aligned} 1,000 &= 10^3 \\ 10,000 &= 10^4 \\ 100,000 &= 10^5 \end{aligned}$$

The value of each digit equals the digit symbol multiplied by 10 to its appropriate power; thus, as indicated in the previous example, the digit 5 in $9,583 = 5 \times 10^2 = 5 \times 100$, while the $9 = 9 \times 10^3$, and so forth. Therefore, when a number is expressed in decimal notation, it is expressed in terms of the sum of various multiples of 10. Ten is said to be the base of this system because of the role that the powers of 10 and the digits of the ten play in the above expansion.

Binary System

The base of the binary system is two. This means that all numbers are expressed in terms of powers of two. Therefore, the understood multipliers, are 2^0, 2^1, 2^2, 2^3, etc. rather than 10^0, 10^1, and 10^2, etc. as in the decimal system. The base 2 implies that only two symbols may be used. Although any two symbols could be selected, it has been common practice to use the symbols of 0 and 1. The symbol '0'normally represents the quantity of 'none'. Therefore, in counting, after one object has been counted, there are no additional symbols to use. As in the decimal system, combinations of symbols must be used to represent higher values. Since it is impossible to have any symbol greater than '1' in any position, the binary system is unique and is of particular value to computers. There can only be two states or conditions in any position of a number, a '0' or a '1'. In addition, there is a carry-over with every second count. Therefore, simple bi-stable (2 state) devices may be employed to count and to provide carry-over pulses.

Practically all physical phenomena are bi-stable. For example, a switch is either on or off, a vacuum tube is either conducting or non-conducting, a magnetic core is polarized in either one direction or the other, an electric pulse is either present or absent, a transistor is either forward or reverse biased, and a relay is either energized or de-energized. When the device is operated, or is considered to be on, it may be described by the symbol '1'; when it is off, or unoperated, it may be described by the symbol '0'.

The following example shows a number in a binary counter. 1 0 1 1 0 The symbol in the right-hand position tells us that there are no 'one's' (0×2^0) while the symbol immediately to its left indicates there is one '2' (1×2^1). The next position tells us that there is one '4' (1×2^2), and the next shows no '8's' (0×2^3). The left-most position in the counter indicates there is one '16' (1×2^4). The whole counter is valued at $16 + 0 + 4 + 2 + 0 = 22$ in the decimal system. Note that for each position in a decimal system there may be any one of ten symbols. In thebinary counter, as above, there can be only two symbols. The following example illustrates how the multipliers are used in conjunction with the value of each position:

$$22 = 16 + 0 + 4 + 2 + 0$$

$$22 = (1x2^4) + (0x2^3) + (1x2^2) + (1x2^1) + (0x2^0)$$

Binary System (continued)

The number of positions in a decimal system are referred to as the number of digits. In the binary system, the positions are referred to as the number of bits. If only the co-efficients of the powers of 2 are written, the binary representation of 22 becomes 10110. Because the binary representation of a number requires only the 2 symbols '0' and '1', the binary system lends itself naturally to the use of core memory, trigger circuits, and so on. These devices can be used to greater advantage and efficiency with the binary system than with the decimal.

Octal

The base of the octal system is 8. This implies that there are only 8 symbols: 0, 1, 2, 3, 4, 5, 6 and 7. It also means that all numbers are expressed as powers of 8. The understood multipliers, are 8^0, 8^1, 8^2, 8^3, 8^4, etc., rather than 10^0, 10^1. 10^2, etc., as in the decimal system.

When counting in the octal system, there are no more symbols to use when the count has reached 7. Therefore, the quantity which is one greater than 7, that is '8', must be made up of a combination of 2 symbols; a '1' and a '0'. As in the decimal system, the one means that the number of symbols available have been exceeded and the zero means that count has stopped after exceeding the number of symbols. However, '10' now represents the eighth count rather than the tenth. Nine, obviously, is now represented by '11' which is one more than '10'. In a two digit octal number, either digit may be as high as 7. If the digit on the left is 7, this means that the counting has proceeded through the 8 available symbols seven times. The following example shows a counter containing digits representing a number in the octal system.

7	5	6	3

The 3 in the right hand position equals (3×8^0), or 3; the 6 in the position to the left of 3 equals (6×8^1) or 48; the 5 in the position to the left of the 6 equals (5×8^2) or 320; and the 7 in the left hand position is equal to (7×8^3) or 3,584. The whole counter is valued at 3,584 + 320 + 48 + 3 or 3,955 in the decimal system.

$$3{,}955_{10} = 7 \times 8^3 + 5 \times 8^2 + 6 \times 8^1 + 3 \times 8^0$$

$$3{,}955_{10} = 7 \times 512 + 5 \times 64 + 6 \times 8 + 3 \times 1$$

$$3{,}955_{10} = 3{,}584 + 320 + 48 + 3$$

Octal (continued)

Remember that an octal number cannot have a symbol of a value higher than 7 in any digit position.

CONVERSION OF NUMBERS

Since the 6400 computer uses a decimal input but stores the number entered, in binary form, it may be necessary to be able to convert from the decimal system to the binary system. It may also be necessary to reverse the procedure and be able to convert from the binary system back into the decimal system.

Decimal to Binary

Decimal numbers are converted to binary numbers by repeated division. Successive division by 2 shows how many times 2^n is contained in the decimal number. The remainder after each division is the number of units left over, after having counted to 2^n. When the remainders obtained in the divisions by 2, are listed in reverse order, the binary equivalent of the decimal number has been found.

$$724_{10} + ?_2$$

724 ÷ 2 = 362 remainder is 0
362 ÷ 2 = 181 remainder is 0
181 ÷ 2 = 90 remainder is 1
90 ÷ 2 = 45 remainder is 0
45 ÷ 2 = 22 remainder is 1
22 ÷ 2 = 11 remainder is 0
11 ÷ 2 = 5 remainder is 1
5 ÷ 2 = 2 remainder is 1
2 ÷ 2 = 1 remainder is 0
1 ÷ 2 = 0 remainder is 1

Therefore, $724_{10} = 1011010100_2$. There are 3 digits in 724_{10} and 10 bits in the binary equivalent. In general, there are three and one-third binary bits for every decimal digit in equivalent numbers. The 6400 computer uses 34 bit words which are approximately equivalent to 10 decimal digits.

Binary to Decimal

To convert a number of its equivalent form in a higher base system, it is easiest to multiply the value of each

Binary to Decimal (continued)

digit position by the digit symbol and add the results. As an example:

$$11100110_2 = ?_{10}$$

$$(1 \times 2^7) + (1 \times 2^6) + (1 \times 2^5) + (0 \times 2^4) + (0 \times 2^3) + (1 \times 2^2) +$$

$$(1 \times 2^1) + (0 \times 2^0) = ?_{10}$$

By rewriting the above example in the following manner and finding the sum of the individual products, the binary number is converted to the base 10.

$$\begin{aligned}
1 \times 2^7 &= 1 \times 128 = 128 \\
1 \times 2^6 &= 1 \times 64 = 64 \\
1 \times 2^5 &= 1 \times 32 = 32 \\
0 \times 2^4 &= 0 \times 16 = 0 \\
0 \times 2^3 &= 0 \times 8 = 0 \\
1 \times 2^2 &= 1 \times 4 = 4 \\
1 \times 2^1 &= 1 \times 2 = 2 \\
0 \times 2^0 &= 0 \times 1 = 0 \\
\hline
\text{Total} &= 230
\end{aligned}$$

Therefore -

$$11100110_2 = 230_{10}$$

Decimal to Octal

The two previous paragraphs illustrate the methods to convert numbers in the base 10 to the equivalent in the base 2 or binary system and from the binary system back into the equivalent in the base 10 or decimal system. This is a rather clumsy and awkward, time-consuming process. The octal system and the binary system have a very unique correlation, which makes it easy to convert from the octal system to the binary system or vice-versa. However, in order to convert from octal to binary or vice-versa, it would be necessary to convert from decimal into octal.

Decimal numbers are converted to octal numbers by repeated division, this being much the same process as was used to

Decimal to Octal (continued)

convert from decimal to binary. In this case, the successive divisions are made with eight being used as the divisor. This will determine how many times 8^n is contained in the decimal number. Each remainder is the number left over after counting to 2^n. Again, the remainders are written in reverse order, which provides the octal equivalent of the decimal number.

As an example:

$$724_{10} = ?_8$$

$$\begin{aligned} 724 \div 8 &= 90, \text{ remainder } 4 \\ 90 \div 8 &= 11, \text{ remainder } 2 \\ 11 \div 8 &= 1, \text{ remainder } 3 \\ 1 \div 8 &= 0, \text{ remainder } 1 \end{aligned}$$

Therefore, $724_{10} = 1,324_8$; there are three digits in 724_{10} and four digits in its octal equivalent. Also note that it only took four divisions to reduce the dividend or the number in the base 10 to zero. Referring back to the decimal to binary conversion paragraph, it stated that there were ten digits required to represent 724 in its binary equivalent and 10 divisions were necessary. It is therefore apparent that it is much less effort to convert from the base 10 into the base 8 than from the base 10 to the base 2. The following paragraph will illustrate the unique feature between the octal and the binary systems.

Octal to Binary

Octal to binary conversion is extremely simple. Because 8 equals 2^3, the conversion can be carried out merely by replacing the octal digits with their binary equivalents, expressed as a three bit binary number. For example, to to convert the octal number 1, 324, simply replace the four with 100, the 2 with 010, the 3 with 011, and the 1 with 001, and obtain 1011010100_2 omitting the 0's on the extreme left.

It can be seen that one of the greatest advantages of the octal system is that it provides a convenient shorthand notation for the binary system. A number in the octal form

Octal to Binary (continued)

is much easier to write since it also required much less space. Also, it provides a better concept of the magnitude of the number.

Binary to Octal

In order to convert the number in the binary system into the octal system, group the binary bits by 3's, beginning from the right. If the last group of three, that is the lefthand group, does not contain 3 full bits, then it is only necessary to add as many zero's as necessary to make a full group of three.

$$001\ 011\ 010\ 100_2$$
$$001/011/010/100_2$$

To obtain the octal equivalent of the binary number, all that is necessary is to write directly below each group of three of the binary number, the decimal equivalent. Writing the decimal equivalent for each group of three of the binary number, gives the octal value.

As an example:

$$001/011/010/100_2$$
$$1\quad 3\quad 2\quad 4_8$$

Therefore, the binary number $1011010100_2 = 1,324_8$. It can be seen from the above example that the left group of the 3 is equal to one, the second group is equal to 3, the third group is equal to 2, and the fourth group of the 3 is equal to four.

This paragraph and the preceding paragraph illustrates the ease of conversion from the octal system to the binary system and from the binary system back into the octal system. Therefore, if it is necessary to know what the binary equivalent of a decimal number is, the best way to convert from decimal to binary is first - to convert the decimal number to its equivalent octal number. Then, convert the octal number into its equivalent binary number. Or if it is necessary to find the decimal equivalent of a

Binary to Octal (continued)

binary number, the procedure can be reversed. The method to convert from the octal system back into decimal is discussed in the next paragraph.

Octal to Decimal

Octal to decimal conversion is accomplished in the same manner as is binary to decimal conversion. Multiply the value of each digit position by the digit symbol and add the products.

As an example:

$$1{,}324_8 = ?_{10}$$

$$(1 \times 8^3) + (3 \times 8^2) + (2 \times 8^1) + (4 \times 8^0) = ?_{10}$$

$$1 \times 512 = 512$$
$$3 \times 64 = 192$$
$$2 \times 8 = 16$$
$$\underline{4 \times 1 = 4}$$

$$\text{Total} = 724_{10}$$

Therefore, $1{,}324_8$ is equal to 724_{10}

The decimal values of the binary bits are listed in the following table.

Bit Position	2^n	n
1	1	0
2	2	1
3	4	2
4	8	3
5	16	4
6	32	5
7	64	6
8	128	7
9	256	8
10	512	9
11	1024	10
12	2048	11
13	4096	12
14	8192	13
15	16384	14

Octal to Decimal (continued)

Bit Position	2^n	n
16	32768	15
17	65536	16
18	131072	17
19	262144	18
20	524288	19
21	1048576	20
22	2097152	21
23	4194304	22
24	8388608	23
25	16777216	24
26	33554432	25
27	67108864	26
28	134217728	27
29	268435456	28
30	536870912	29
31	1073741824	30
32	2147483648	31
33	4294967296	32
34	8589934592	33
35	17179869184	34

BINARY ARITHMETIC OPERATION

As previously stated, binary numbers in general have more terms than their decimal counterparts (on an average about 3.3 times as many), and arithmetic operations in the binary system becomes quite simple.

Addition

The rules for adding binary bits are as follows:

0 + 0 = 0
1 + 0 = 1
0 + 1 = 1
1 + 1 = 10 (zero with a carry)

The answer to the last line of the above set stated that 1 + 1 equals 10. This means that this generated a carry over to the next high order position.

Addition (continued)

As an example, add 1111011 to itself:

carries	1111 11	123_{10}
	1111011_2	123_{10}
	$+1111011_2$	246_{10}
	11110110_2	

Subtraction

The rules for subtraction are as follows:

0 - 0 = 0
1 - 1 = 0
1 - 0 = 1
0 - 1 = 1 with a borrow

As an example, subtract 1111011 from 11110110

Borrows	1111 11	246
	11110110	-123
	-01111011	123
	01111011	

Multiplication

The multiplication table for binary bits is as follows:

0 x 0 = 0
1 x 0 = 0
0 x 1 = 0
1 x 1 = 1

The rules for carrying out multiplication and division in longhand are similar to those used with the decimal system.

For example, the multiplication of 111 by 101 is done as follows:

111	7
x101	x5
111	35
000	
111	
100011	

Multiplication (continued)

It is evident that multiplication performed in the above longhand system is identical to that of the decimal system. That is, the rules of multiplication are used for each bit position of the multiplier, then the partial products are added together for the total product.

COMBINATIONAL LOGIC

LOGICAL OPERATIONS

An electronic computer requires circuits capable of making logical decisions when combinations of these circuits are connected in a logical manner. The output of these logic circuits will be a voltage or current pulse that will be construed as either a YES or NO answer, depending on the logical significance of inputs to the logic circuit. There are only two basic types of logical functions that must be performed by logic circuitry, AND and OR functions.

In computer design it is possible to design the majority of the necessary circuitry for a given computer by using only AND and OR gates or switches. There are a number of special circuits required to control the gate inputs, but these special circuits represent a small percentage of the total volume of circuits. The major complexity of a computer is due more to the manner of interconnecting the logic gate circuits than due to the logic circuit designs in themselves. The AND and OR functions can be implemented with diodes, relays, tubes, and transistor circuits. This discussion does not cover the various circuit components, but strives to present the logical operation they perform regardless of type.

"AND" FUNCTION

An "AND" function is a logical device that consists of a number of inputs and one output. To describe its logical function, it can be stated that if all of the inputs are at their active (Yes, On, Up, etc.) state, the output will be at its active state. If any one of the inputs is at its inactive (No, Off, Down, etc.) state, the output is at its inactive state.

"AND" FUNCTION (continued)

Consider an "AND" function with only two inputs, the logic symbol is shown in Figure 1-1

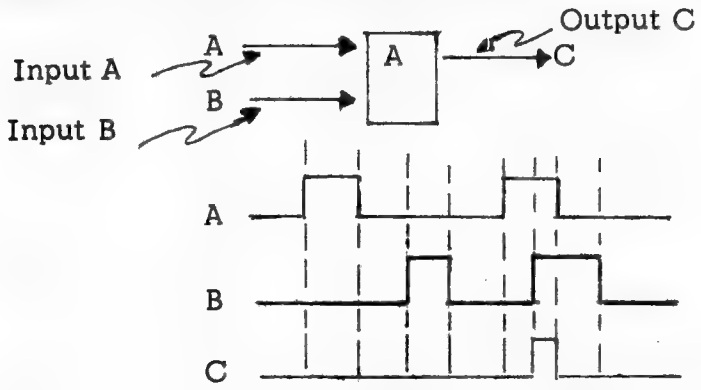


FIGURE 1-1 "AND" FUNCTION

This logic function is referred to as several things, namely, "AND" Gate, "AND" Switch, and an "AND" Circuit. To illustrate the logic performed by the "AND" function, the following example is used.

A "YES" output will be obtained for only Thanksgiving Day when all of the input conditions have been met. The input conditions consider the month, the week of the month, and the day, Figure 1-2.

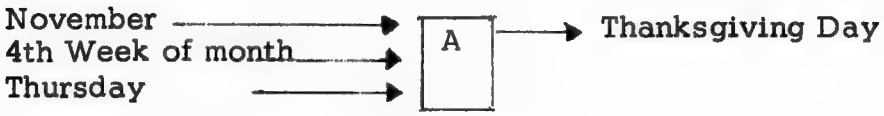


FIGURE 1-2. Example of AND Function

This can also be further illustrated in a Timing Chart, Figure 1-3

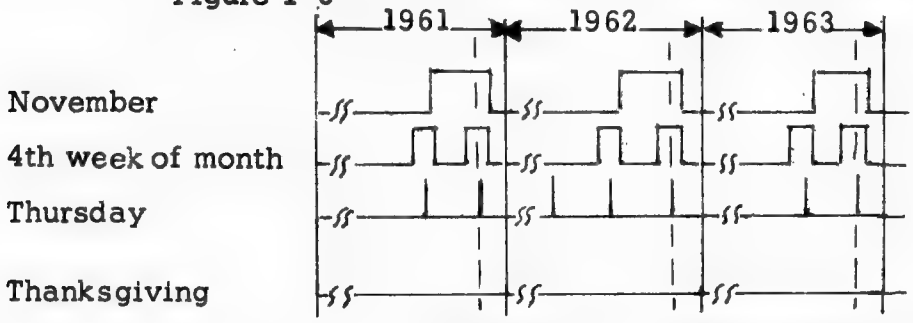


FIGURE 1-3. Training Chart of an AND Function

"OR" FUNCTION

An "OR" function is similar to the "AND" function insofar as the "OR" function is a logical device that also consists of a number of inputs and one output. However, there are 2 types of "OR" functions that are used in the SABA unit, that should be defined. The most common and most often referred to "OR" function is called an "Inclusive OR". The other "OR" function is called an "Exclusive OR".

Inclusive "OR"

The logic performed by an "Inclusive OR" is such that in order to obtain an active output, any one of the inputs must be active.

Consider an "OR" function with only 2 inputs, A and B, in Figure 1-4

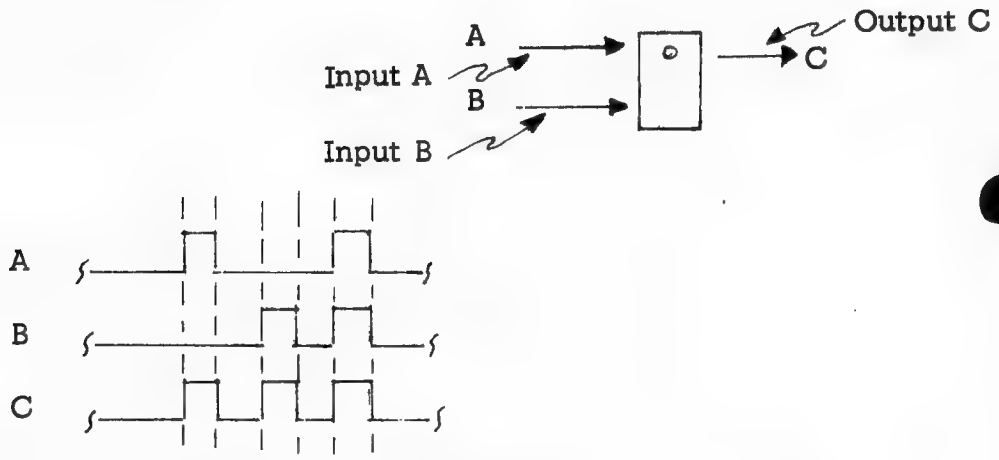


FIGURE 1-4. "OR" Function

If either A or B, or both, are at an active level, then the output is at an active level. If both inputs are inactive or unconditioned, then the output is inactive. The following example, Figure 1-5, further explains the "OR" function.

Inclusive "OR"(continued)

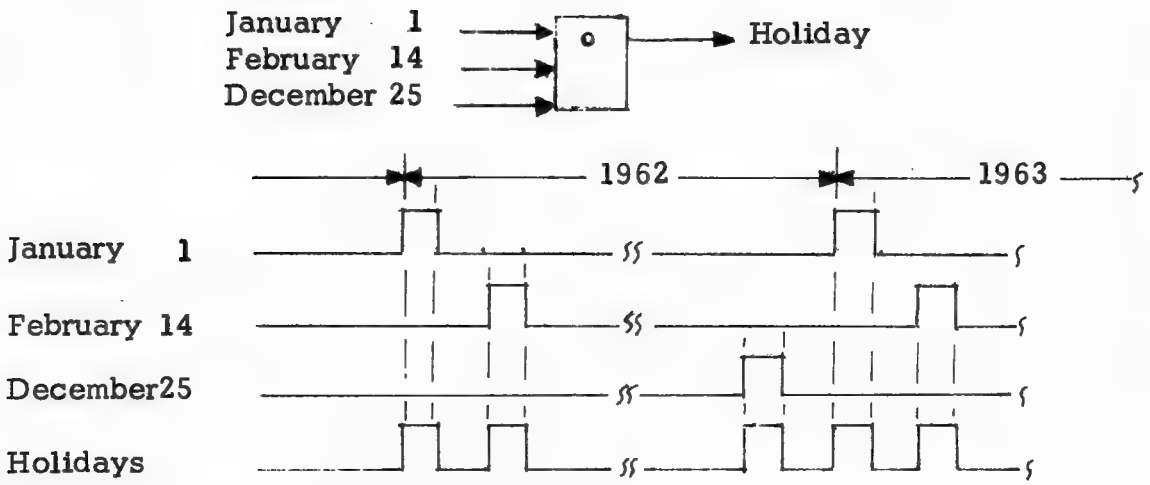


FIGURE 1-5. Example of OR Function

A holiday is generated any time a January 1, February 14, or December 25 appears at one of the inputs.

Exclusive "OR"

An exclusive "OR" function is an "OR" function with specific stipulations concerning the inputs. The output of an exclusive "OR" is active only under the 2 following conditions, Figure 1-6

First, if A is active and B is inactive, or second, if A is inactive and B is active, then the output C is active. If both are inactive or if both are active, the output is inactive

The generally accepted symbol for an exclusive "OR" is ∀

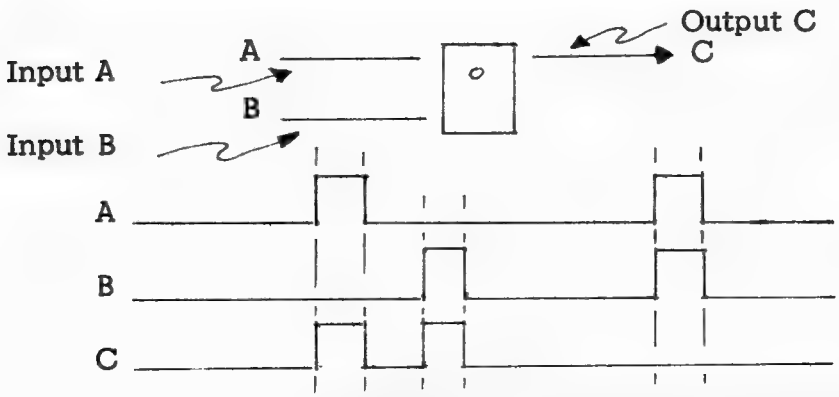


FIGURE 1-6. Exclusive OR function

Exclusive "OR" (continued)

To further illustrate the exclusive "OR" function, consider the following example, Figure 1-7, where the logic output determines when the algebraic sign of a product must be negative. (+ is considered to be an active level, and - an inactive level.)

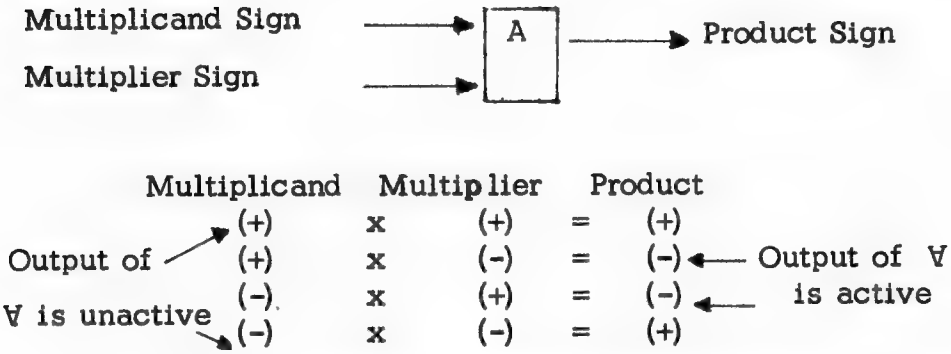


FIGURE 1-7. Example of Exclusive OR function

The function describes the familiar algebraic rules of a multiplication in a convenient form.

Invert

Since a number of devices used to implement the logical "AND" and "OR" functions provide a 180 degree phase shift, it is also necessary to consider the "Invert" function. Also it becomes a very useful logic function when a number of "AND" and "OR" functions are combined.

Figure 1-8 illustrates the invert function.

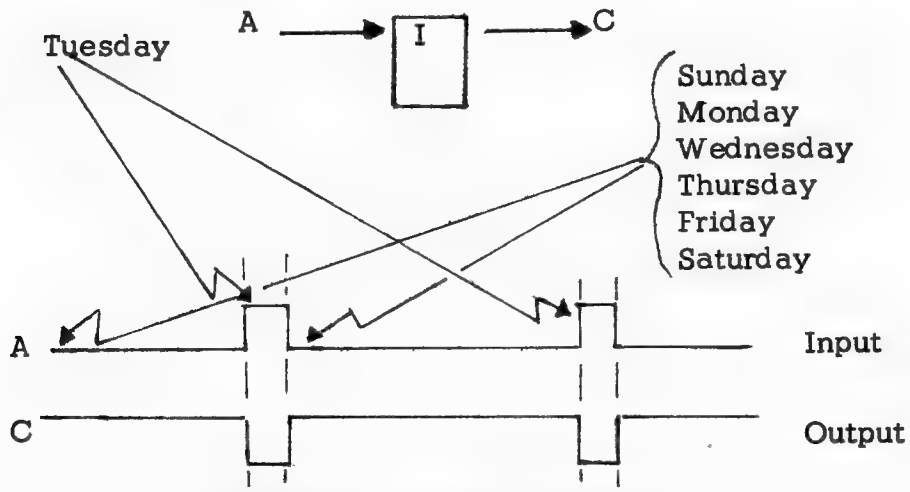


FIGURE 1-8. Invert Function

Invert (continued)

The invert function simply reverses the logic, and depending upon the scope of the input, as in Figure 1-8, the output may be a number of other functions, which could be considered as being "ANDED" together.

AND FUNCTION

Rather than draw a logic block showing inputs and output, a shorthand method of notation is necessary. It also assists to use the shorthand notation when combining various logic functions.

The "AND" function is identified by a dot (.) between terms, Figure 1-9

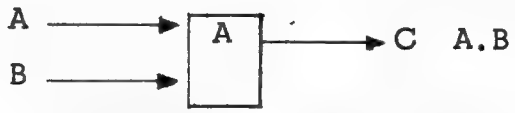


FIGURE 1-9. AND Function Notation

Sometimes the (.) showing the "ANDING" between two function is omitted, but the "AND" function is still implied, Figure 1-10

FIGURE 1-10. AND Function Notation

When several logic functions containing several variables are "ANDED" together, the "AND" function is shown by parenthesis, and is illustrated with 2 variables in Figure 1-11.

FIGURE 1-11. AND Function Notation

"OR" FUNCTION

The "OR" function (inclusive) is identified by a plus (+) between terms, Figure 1-12.

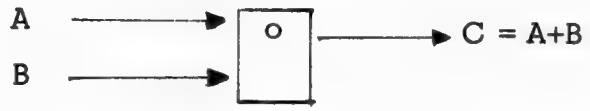


FIGURE 1-12. OR Function Notation

INVERT FUNCTION

The notation used to show that an invert function is used, is a bar drawn over the function that has been inverted, Figure 1-13.

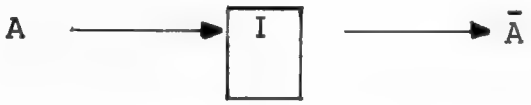


FIGURE 1-13. Invert Function Notation

When a bar over the function is used, it is said that the function is inverted, notted, or complemented. Also, when discussing bi-stable devices (triggers), the bar is used to show the "OFF" output, as the device usually has both "ON" and "OFF" outputs.

With these three logic notation symbols, the ., + and $^{-}$, it is possible to express any logic function in the shorthand method.

In describing the input and output states of logic functions, it becomes necessary to define the various statements or words used that show active or inactive conditions. If the logic function is in the active state, it can be ON, conditioned, at a plus level, a logic 1 or 1 state, Yes, True, and Up.

If the function is inactive, the inactive state can be OFF, unconditioned, at a minus level, a logic 0 or state, No, Untrue, and Down.

COMBINED FUNCTIONS

In order to perform the logical decisions necessary in a computer, "AND" and "OR" functions are combined in various arrangements. To illustrate the need for Combinational Logic, consider the case of the exclusive "OR" function, Figure 1-14.

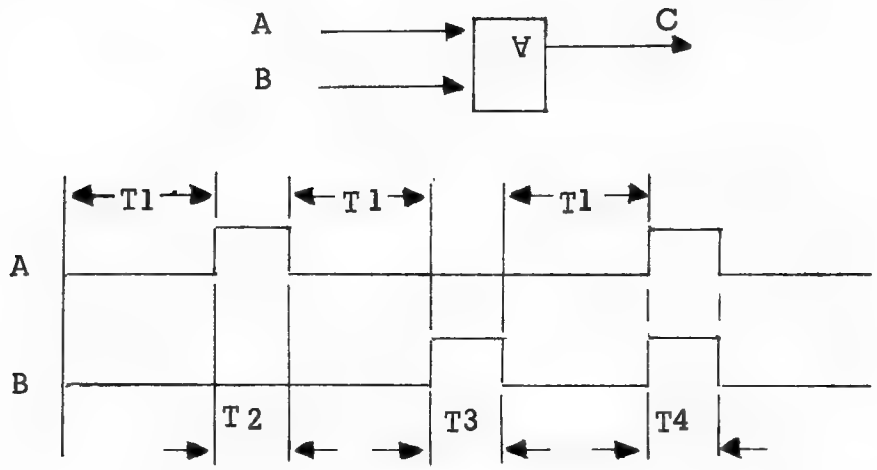


FIGURE 1-14. Exclusive OR Function Timing Chart

The exclusive "OR" function states that in order to obtain an active output C, either input A or B must be at an active level, but not both, and with both inactive, the output is inactive. Therefore, periods T2 and T3 should produce active outputs, and T1 and T4 inactive outputs.

In order to perform this function in "AND" and "OR" terms, it is necessary to consider each state of the input functions.

During periods T1, the inputs A and B are unconditioned, therefore the output must be unconditioned in order to perform ∀logic. In period T2, input A is true and B is untrue; and during period T3, input A is untrue and B is true. For both periods T2 and T3 an up or conditioned output is desired. During period T4, both inputs are true and for an ∀ function, this must produce a down or unconditioned output.

There are four different situations, two that will provide a conditioned output and two that provide an unconditioned

output. Each individual situation considers the state of two variables, A and B. Since only two of the situations provide a conditioned output, the logic for these two conditions must be implemented in some form.

Figure 1-15 shows two "AND" switches that generate these two conditions.

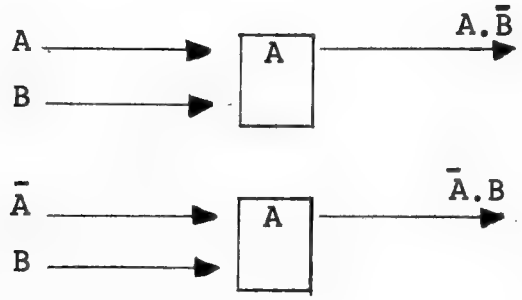


FIGURE 1-15. Partial Logic of Exclusive OR Function

Inputs A and $\bar{B}$ generate $A.\bar{B}$, inputs $\bar{A}$ and B generate $\bar{A}.B$. Since the ∀ function calls for either of these two conditions, then the ∀ function can be implemented if the outputs of the two "AND" switches are "ORED" together, Figure 1-16.

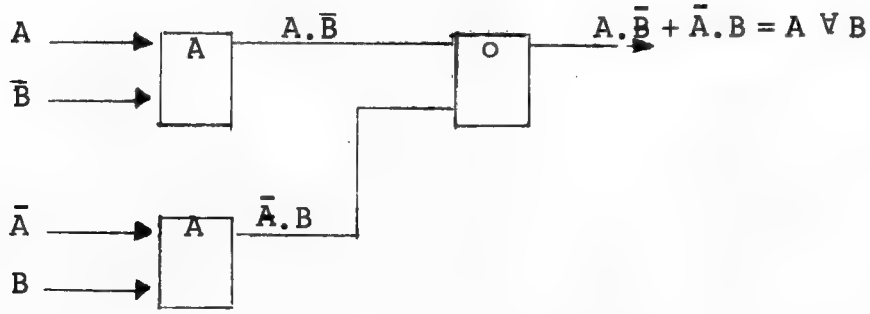


FIGURE 1-16. Logic For Exclusive OR Function

The discussion of the ∀ function has shown the way that individual "AND" and "OR" functions are combined to provide over-all functions.

Another aspect of combination logic is that there are normally a number of different logic circuit arrangements that accomplish the same over-all function. As an example, the ∀ function can be implemented with "AND" and "OR" circuits as in Figure 1-17.

The timing diagram in Figure 1-17 illustrated how the two "OR" functions "ANDED" together will also produce the ∀ functions. Another point of combinational logic should be observed, that is that with more than one way to implement a function, there may be considerable difficulty in interpreting the various parts of the logic function.

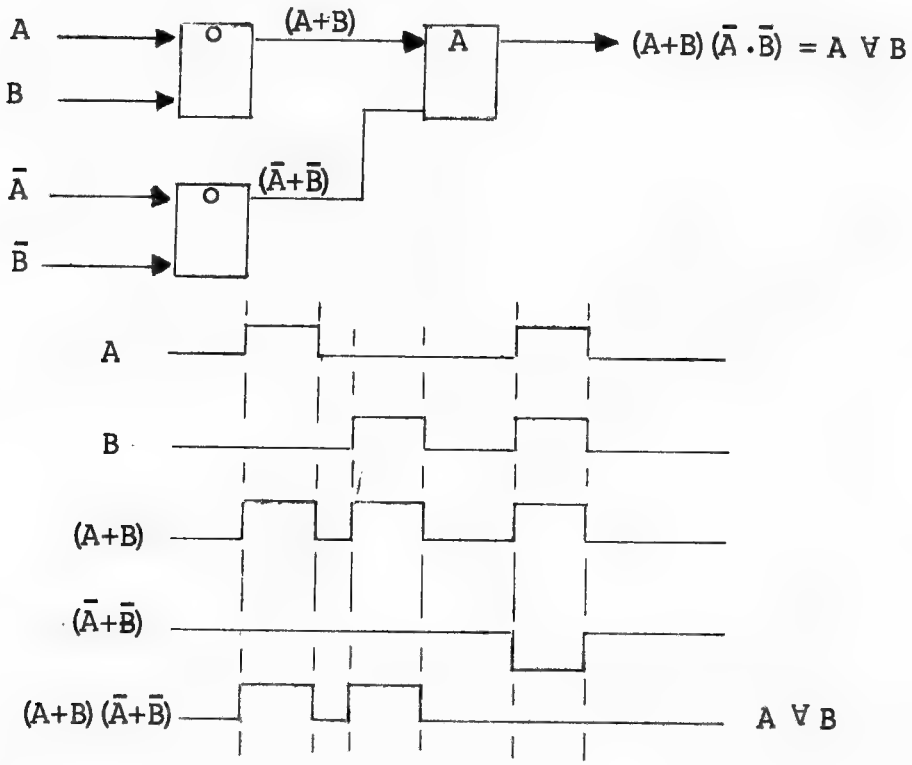


FIGURE 1-17. Logic & Timing Chart for Exclusive OR Function

Take, for example, the two expressions for the ∀ function, $A.\bar{B} + A.B$ and $(A+B)\ (\overline{A+B})$. The expression with the two "AND" functions "ORED" is much easier to identify as far as the various possible states of the variables A and B than the other expression. In general, it is more difficult to

to interpret "OR" functions, "ANDED" together. It is possible to change the expression and assist the interpretation. This is done by expanding the expression, although the original construction logic is lost. In the following example the two OR functions are, in effect, multiplied together, Figure 1-18.

$$
\begin{array}{r}
(A + B) \\
(\bar{A} + \bar{B}) \\
\hline
+A\bar{B} + B\bar{B} \\
A\bar{A} + \bar{A}B \\
\hline
A\bar{A} + \bar{A}B + A\bar{B} + B\bar{B}
\end{array}
$$

FIGURE 1-18. Multiplying Two OR Functions together

When the expression is expanded, there are four terms, two new ones, and two that are the same as the first example of an $\forall$,Figure 1-16 Consider the two new terms $A\bar{A} + B\bar{B}$. If an "AND" logic switch with 2 inputs, one with A and the other with $\bar{A}$, the output will always assume an unconditioned state. This is true because a device capable of being in one of two states (A or $\bar{A}$) cannot logically ever satisfy the "AND" function A.A. Since this term is an impossibility, it is equal to zero. Therefore the two terms $A.\bar{A} + B.\bar{B}$ are equal to zero and the expression becomes $A.\bar{B} + \bar{A}.B$, which of course is the original concept, even through it directly represents the logic $(A+B)(\bar{A}+\bar{B})$.

The above discussion relates the fact that if the expression for a particular logic function is written, it is possible to find a more recognizable expression which is in effect equal to the original expression.

Since there is a varied amount of circuit components that can be used to implement the two basic logic functions, the type of component used may determine the combinations of functions used.

INVERSION OF FUNCTIONS

Many times computer logic requires the inversion of a combinational function. It is helpful to be able to invert the function in the shorthand notation and further, perhaps to simply the inverted function.

When one variable is inverted, a bar is drawn over the top such as in Figure 1-19.

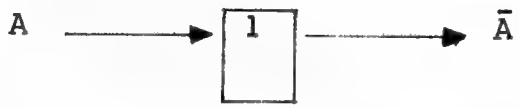


FIGURE 1-19. Bar Notation

To do this, the only action required is to draw the bar over the variable.

However, when more than one variable is involved, it is necessary to change the function as well as inverting each variable. For example, Figure 1-20 shows the complementing of the two terms of ∀ function.

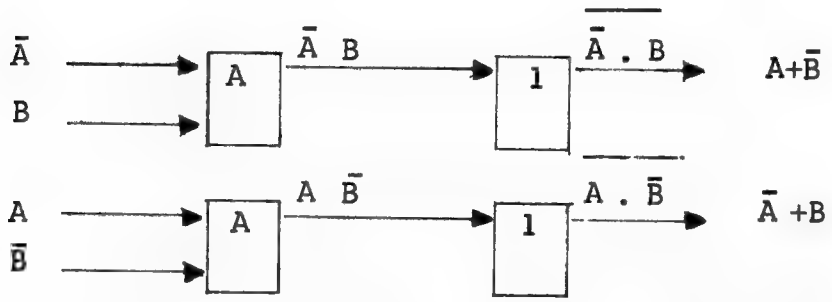


FIGURE 1-20. Complementing Terms of Exclusive OR Function

The above example shows that there are two steps to inverting a function or complementing. First the variable is inverted and second the function is changed, that is the +'s are changed to dots (.) and the dots (.) are changed to +'s.

To further illustrate the method of complementing Figure 1-21 continues from Figure 1-20.

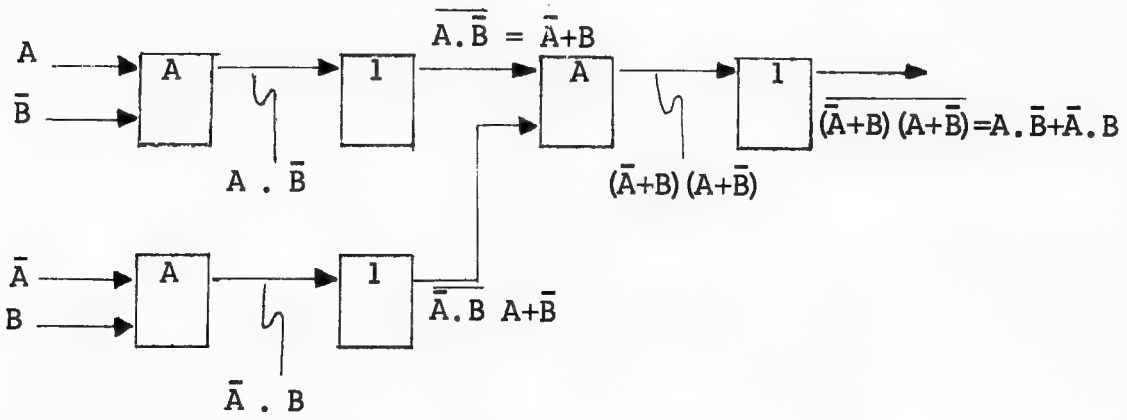


FIGURE 1-21. Method of Complementing a Function

In Figure 1-21, the two terms that were inverted in Figure 1-20 are used as inputs to a 3rd "AND" switch, of which its output is inverted, generating the A function. This illustrates the inversion of a function that includes parenthesis.

To summarize the method of inverting a combinational logic function the following example is used.

$$f = \bar{A}.B(C+\bar{D}) + \overline{A.B.C} + \bar{D}$$

The above function is represented in "AND" and "OR" logic by the following illustration, Figure 1-22

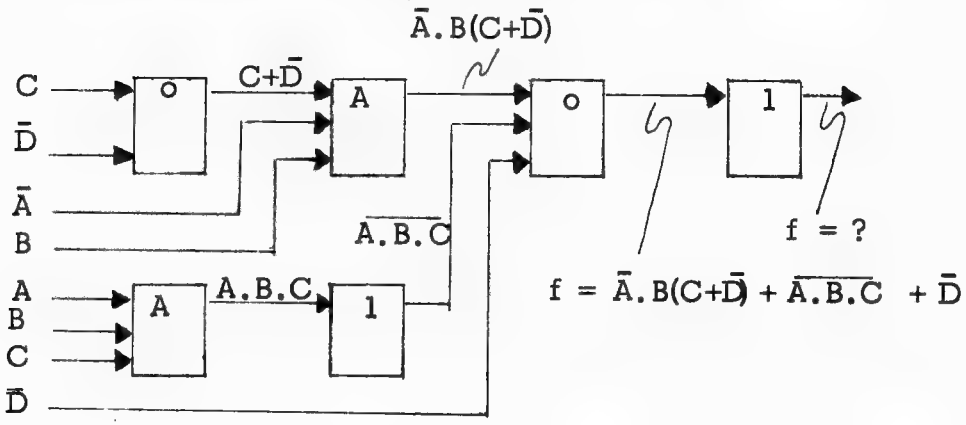


FIGURE 1-22. Complementing the Output of Combinational Logic

It can be seen that it would be difficult to visualize what $\bar{f}$ should be. This example does not necessarily represent a typical logic group, but only serves to illustrate the method of inverting a combinational logic function.

The first step is to rewrite the function with a bar over the entire notation.

$$\bar{f} = \overline{\bar{A}.B.\ (C+\bar{D}) + A.B.C + \bar{D}}$$

Now regroup the major "OR" functions, and change the +'s to .'s, thus eliminating the bar over the entire notation.

$$\bar{f} = [\overline{\bar{A}.B.\ (C + \bar{D})}] \ . \ [\overline{\overline{A.B.C}}] \ . \ [\bar{\bar{D}}]$$

Proceed in complementing each individual function, by complementing each variable and changing the signs. Since the last two functions $[\overline{\overline{A.B.C}}]$ and $[\bar{\bar{D}}]$ are doubly inverted, it is only necessary to remove the 2 bars.

$$\bar{f} = [A + \bar{B} + (\bar{C}.D)] \ . \ [A.B.C] \ . \ [D]$$

Now it is clear that some of the parenthesis and brackets can be eliminated, without altering the expressing.

$$\bar{f} = (A + \bar{B} + \bar{C}.D) \ . \ A.B.C.D$$

Expand the expression.

$$\bar{f} = A.A.B.C.D + A.B.\bar{B}.C.D + A.B.C.\bar{C}.D$$

The first term A.A.B.C.D is equivalently reduced to A.B.C.D as A.A=A, Figure 1-23.

In both the 2nd and 3rd terms, a different situation exists. In the 2nd term $B.\bar{B}$ is a condition that can never occur, or can be considered equal to zero. Therefore $A.B.\bar{B}.C.D = 0$ as well as the last term since $C.\bar{C} = 0$

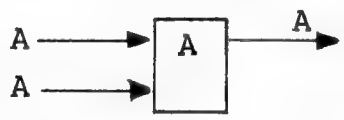


FIGURE 1-23. A Two Input AND Function With Both Inputs the Same

INVERSION OF FUNCTIONS (continued)

The over-all inverted function has been reduced to A.B.C.D, which certainly has rendered it to an extremely simple form and could be very easily identified.

TRUTH TABLES

A logic truth table shows the various states that can exist for any number of variables. It does not show the various "AND" and "OR" combinations that can be used to implement the required logic. It can also show the logic terms required to produce an output for the function as well as show the terms that are not necessary or redundant.

The following example illustrates the use of a truth table. The problem is to have a light be turned on or off from 3 different locations, Figure 1-24.

Figure 1-25 shows the truth table describing the desired action of the light controlled by switches A, B, and C.

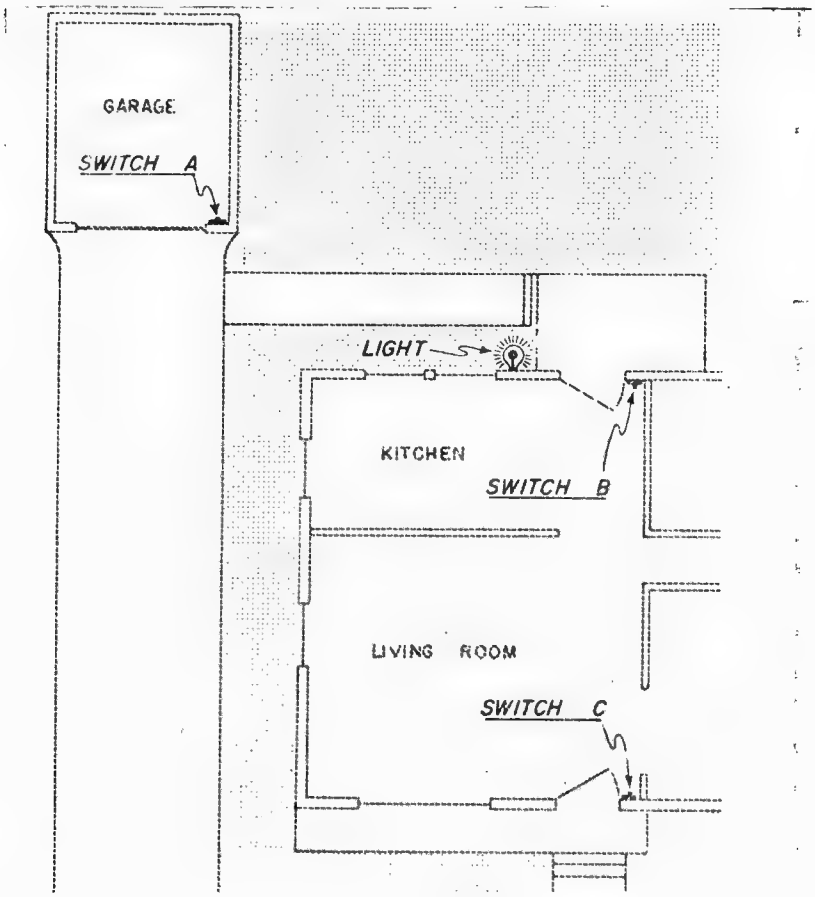


FIGURE 1-24. Truth Table Problem

The truth table can be used to show the various conditions that will be present in the problem described. For the starting situation, assume that all switches are OFF.

	SW A	SW B	SW C	LAMP
① →	OFF	OFF	OFF	OFF

Switch A	Switch B	Switch C	Light
OFF	OFF	OFF	OFF
ON	OFF	OFF	ON
OFF	ON	OFF	ON
OFF	OFF	ON	ON
ON	ON	OFF	OFF
OFF	ON	ON	OFF
ON	OFF	ON	OFF
ON	ON	ON	ON

FIGURE 1-25. Truth Table

If switch A is turned on, then the lamp should be lit.

	SW A	SW B	SW C	LAMP
	OFF	OFF	OFF	OFF
② →	ON	OFF	OFF	ON

Of course if switch A should be turned off, then the lamp would be OFF. However if A were left on and the lamp was to be turned off from another location, say B, the following situation occurs.

	SW A	SW B	SW C	LAMP
	OFF	OFF	OFF	OFF
	ON	OFF	OFF	ON
③ →	ON	ON	OFF	OFF

Again, if switch B were turned off, the situation would revert to 2 . Now, if switch C is operated, the lamp should be turned ON.

	SW A	SW B	SW C	LAMP
	OFF	OFF	OFF	OFF
	ON	OFF	OFF	ON
	ON	ON	OFF	OFF
④ →	ON	ON	ON	ON

The process can continue until all possible combinations have been utilized turning the lamp ON and OFF, this being shown below.

	SW A	SW B	SW C	LAMP
① →	OFF	OFF	OFF	OFF
② →	ON	OFF	OFF	ON
③ →	ON	ON	OFF	OFF
④ →	ON	ON	ON	ON
⑤ →	OFF	ON	ON	OFF
⑥ →	OFF	ON	OFF	ON
⑦ →	OFF	OFF	OFF	OFF
⑧ →	OFF	OFF	ON	ON
⑨ →	ON	OFF	ON	OFF

With step ⑨, all possible combinations have been used, and step ⑦ being a repeat of 1. It may be easier to visualize the various combinations if the table were re-written, substituting a (0) for OFF and a (1) for ON.

	SW A	SW B	SW C	LAMP
① →	0	0	0	0
	1	0	0	1
	1	1	0	0
	1	1	1	1
	0	1	1	0
	0	1	0	1
⑦ →	0	0	0	0
	0	0	1	1
	1	0	1	0

Now, to further simplify the table, a binary bit value can be assigned to each switch and an additional column added showing the decimal equivalent value for each line, then the lines may be rearranged in sequence. Also since line ⑦ is identical to line ①, line ⑦ can be eliminated, Figure 1-26.

4 Switch A	2 Switch B	1 Switch C	Lamp	Decimal Value
0	0	0	0	0
0	0	1	1	1
0	1	0	1	2
0	1	1	0	3
1	0	0	1	4
1	0	1	0	5
1	1	0	0	6
1	1	1	1	7

FIGURE 1-26. Truth Table in Terms of "0" and "1"

With the table above rearranged, this is the Truth Table. As stated before, it shows all possible combinations, and divides the output (whether the lamp is ON or OFF)in two groups.

This table could be rewritten again, in order to classify the ON or OFF status of the output and in the rewriting, use the shorthand method notation for each line or term.

LAMP OFF	LAMP ON
$\bar{A}.\bar{B}.\bar{C}$	$\bar{A}.\bar{B}.C$
$\bar{A}.B.C$	$\bar{A}.B.\bar{C}$
$A.\bar{B}.C$	$A.\bar{B}.\bar{C}$
$A.B.\bar{C}$	$A.B.C$

To further illustrate the benefit of a Truth Table, an example that follows using switches will be shown to implement the logic with specific hardware. It should be noted that this could also be accomplished with tubes, diodes or transistor circuits.

Since the terms identifying the situations when the light should be ON are known, the switches can be connected to perform the AND and OR logic functions.

First, connect all the AND functions, Figure 1-27

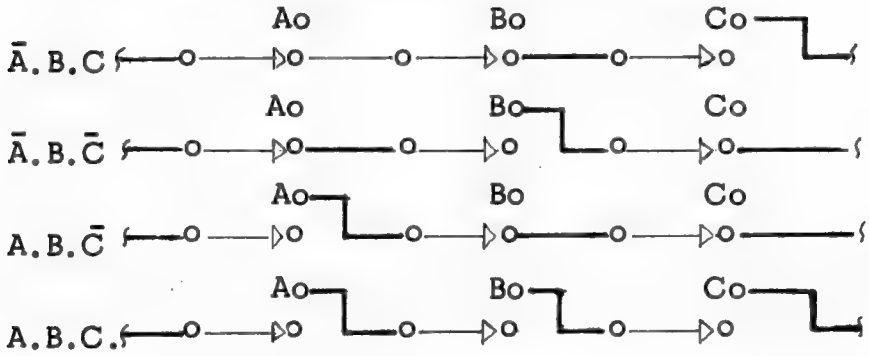


FIGURE 1-27. Expressing Terms of Truth Table with Switches

Each of the switch connection arrangements fulfill the 4 AND functions. Since an OR situation exists between the 4 AND functions, connections must be made for the ORing together.

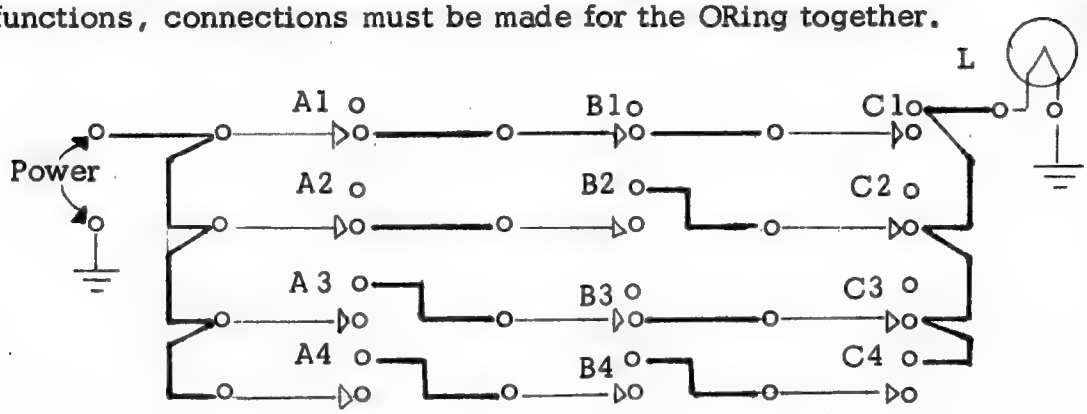


FIGURE 1-28. Complete Circuit Drawn From Truth Table.

Next the lamp and power are connected and our wiring diagram is logically correct. As illustrated in the above sketch, it appears that each switch must have 4 poles. However, on close examination, it is found that some can be eliminated. First look at switch A, Figure 1-29.

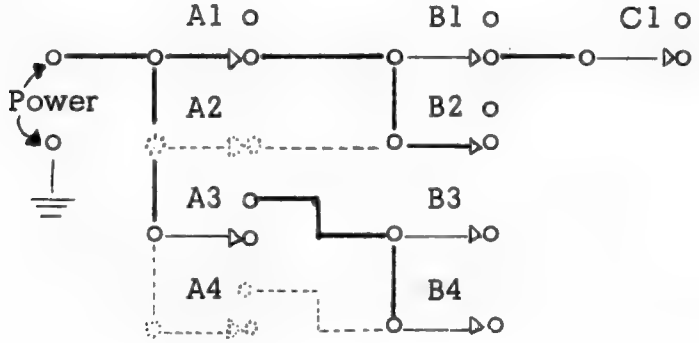


FIGURE 1-29. Removal of Two Positions of A Switch

The switch poles removed are electrically the same. Now notice that both positions of each pole are not used. The switch can be reconnected utilizing both positions, Figure 1-30.

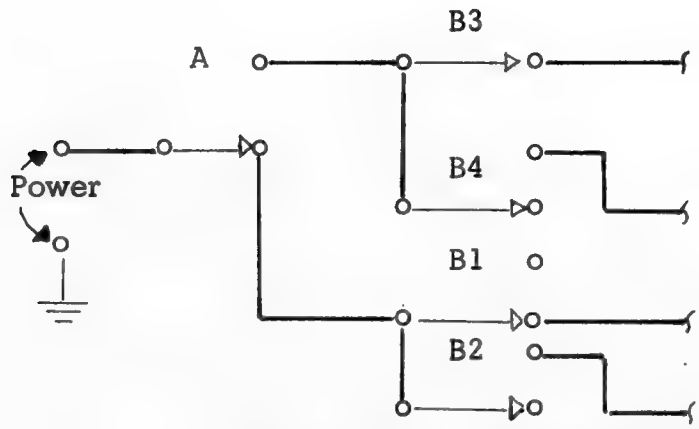


FIGURE 1-30. Completion of A Switch Simplification

Looking back at switch C, it has much of the same configurations as switch A did if all poles were turned backward, Figure 1-31.

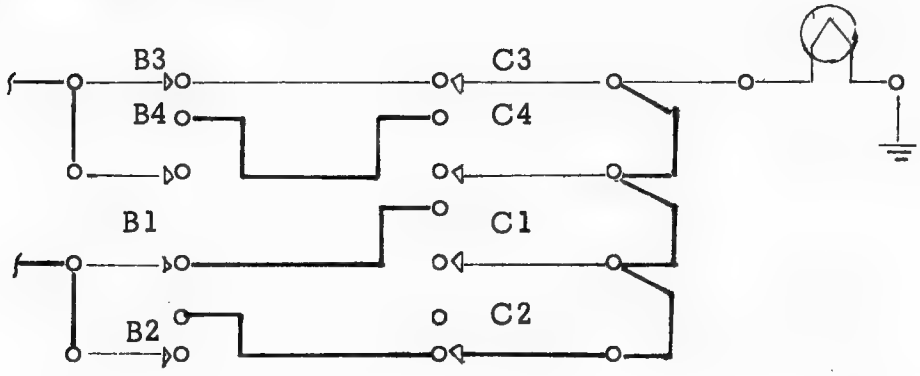


FIGURE 1-31 Re-arrangement of C Switch

Simplifying the switching arrangement of switch C in the same fashion as switch A, the circuit becomes available with 2 poles for switch C, Figure 1-32.

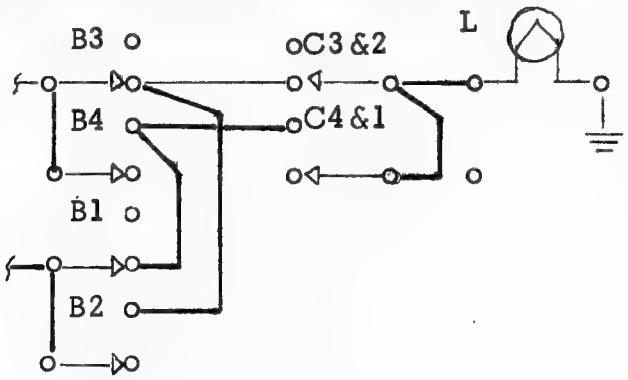


FIGURE 1-32. Removal of Two Positions of C Switch

Now, using both positions of switch C, switch C now only required 1 pole, Figure 1-33.

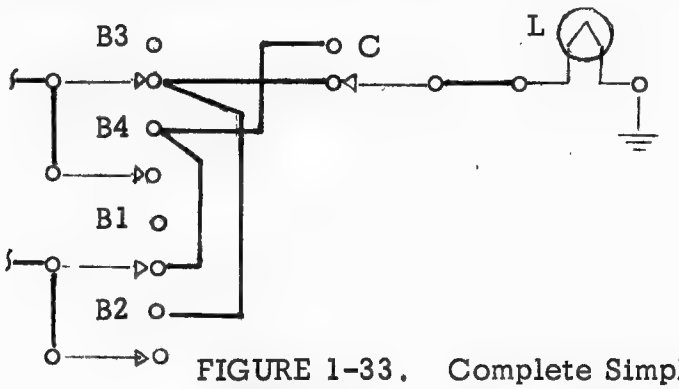


FIGURE 1-33. Complete Simplification for C Switch Logic

It is also now evident that positions 3 and 4, 1 and 2 of switch B can make use of unused terminals, Figure 1-34.

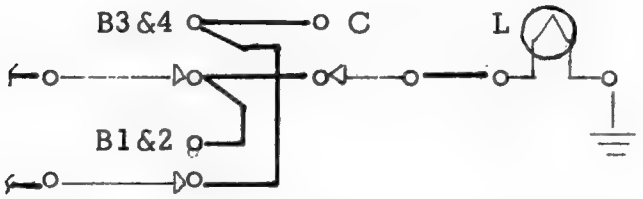


FIGURE 1-34. Simplification of B Switch Connection

Adding switch A and completing the simplified connections, the drawing is complete, Figure 1-35.

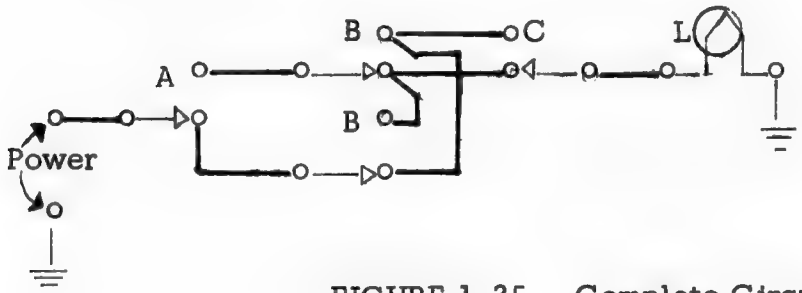


FIGURE 1-35. Complete Circuit After Simplification

There is an additional facet shown by a Truth Table that should be recognized. For example, consider the outputs available from a binary counter that has four memory devices, A,B, C and D. If outputs were required only for values from 0-9 in the counter, a Truth Table shows that the values 10-15 could be present if the counter were allowed to progress beyond 9. If the counter were restricted to containing a value of more than 9, then started to repeat, values from 10-15 could never occur. These situations (10-15) are said to be redundant.

Redundant terms often simplify the logic required to perform a particular operation.

SIGNED ASSYNCHRONOUS BINARY ADDER

CHAPTER 2

SEMI-CONDUCTOR PHYSICS

CHAPTER 2.

SEMI-CONDUCTOR PHYSICS

Atomic Structure

The atom of any element consists of a central mass called the nucleus and one or more electrons in orbit around the nucleus. The nucleus is comprised of neutrons and protrons. The majority of the mass is concentrated in the nucleus, but the electrons in orbit about the nucleus play a large part in determining the chemical and physical properties of the element. The electrons that rotate about the nucleus in orbit, are not in the same plane. However, there is a discrete orbit in which any electron tends to stay under normal conditions. The orbits of these electrons are grouped in bands, and are not necessarily regular and circular.

Considerably more energy must be applied to the atom to remove the electrons from the inner groups or bands, than the outer band, because these electrons are held more tightly by the nucleus. Each group or band can contain a certain maximum number of electrons and when the band contains this number, it is called a filled band. It is easier to move an electron from an unfilled band than it is from a filled band. Since the electrons in orbit about the nucleus fall into bands with discrete maximum numbers in the bands, the gaps between the bands are called forbidden regions. Electrons are not normally found in the forbidden regions. If an electron moves from one band to another, it has jumped the energy gap.

Good conductors have few electrons in their outer bands. Examples of good conductors are gold, silver, and copper. Each of these elements has only one electron in the outer band. The difference in the conducting abilities of each of the above mentioned elements is due, in part, to the distance of the single electron in the outer band from the nucleus.

Atoms that have 8 electrons in the outer band are insulators. The inert gases, neon, argon, and krypton, are examples. The insulator effect is explained by the octet theory. The K,L,M,N,.....bands have orbit capacities of 2,8,18,32,..... electrons still are valid, and that these capacities apply only to the inside orbits, and not to the two outermost orbits.

The outermost orbit can contain only 8 electrons. A give and take situation occurs in which the outer orbit accepts 8 or fewer electrons and the next to the outermost orbit adjusts itself to 18 or 32 or even 8, in order to satisfy the octect condition. An example of this rule is antimony, with an atomic number of 51. The number of electrons per orbit from inner to outer is 2, 8, 18, and 5. The question may arise, why not 2,8,18 and 23. The answer is because the octet theory applies.

When an atom has filled outer band of 8 electrons, it is considered to be in its most stable condition. Because of this fact, it takes a large amount of energy to displace one of the 8 electrons, Figure 2.1, compared to the energy required to displace a single electron that does not have 7 neighboring electrons in another atom. Argon has a filled outer band of 8; therefore, it is a good insulator. Silver has only 1 electron in its outer band, therefore it is a good conductor. Figure 2.2 shows a chart of resistance for conductors, semi-conductors, and insulators.

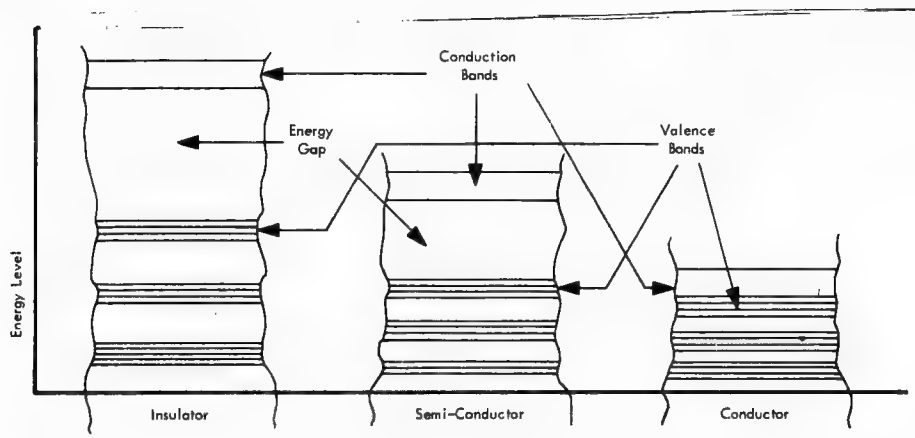


FIGURE 2.1 Comparison of Energy Levels

Co-Valent Bonding

Electrons that rotate in the outermost orbits or the last band of the atom are far removed from the nucleus; in fact, the outer orbits of the electrons of one atom cross the outer orbits of electrons from a neighboring atom. During the course of travel of an electron, it is acted on by its own nucleus and the nuclei of its neighboring atoms, Figure 2.3, so that in germanium, one atom has four of its own electrons in the outer band and feels the effects of electrons from four of its neighboring atoms. The combination is similar to the insulator action described by the octet theory, because there are now eight electrons in an octect relationship about the germanium nucleus and this phenomenon is called "co-valent bonding". The electrons in the outer orbits or band of an atom are said to be in the valence band. Figure 2.4 shows the diagram of this germanium atom.

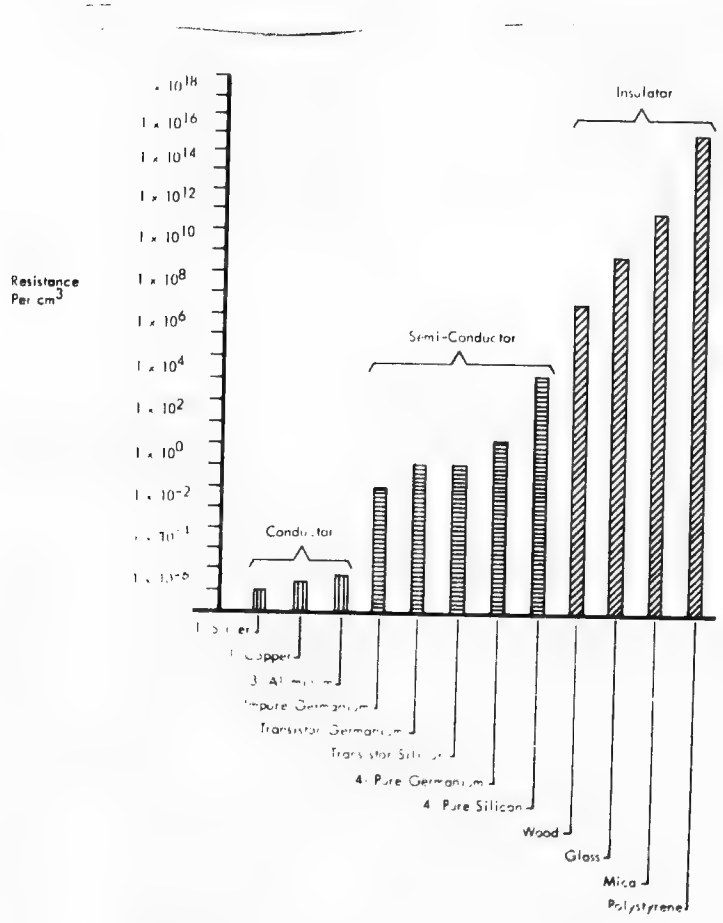


FIGURE 2.2 Resistance of Materials

Co-Valent Bonding (continued)

The balance of energy existing between adjacent valance electrons, determines the geometric arrangement of the atoms. Germanium arranges itself in what is called a diamond lattice network. The co-valent bonding of the four valence electrons of a germanium atom, develops the diamond shaped lattice shown in Figure 2.5. The germanium atom having four electrons in its outer band, is halfway between the minimum number and the maximum number of electrons. It would appear that germanium would have electrical properties somewhere between the conductors and insulators. For this reason, germanium is classified as a semi-conductor. The inner orbit electrons of the germanium atom arrange themselves into bands of 2,8, and 18 electrons. These bands are filled and the outer band having four electrons, is the property of the atom that is necessary to study for an understanding of transistor action. It can also be said that it requires about 15 times as much energy to remove a co-valent bonded electron from the valence band as it does to remove an electron in the valence band that is not in co-valent bonding.

Germanium that is extremely pure or intrinsic has a resistance of about 60 ohms per cubic centrimeter. If an extremely small amount of impurity is added to germanium, the resistance drops to about 4 ohms per cubic centimeter.

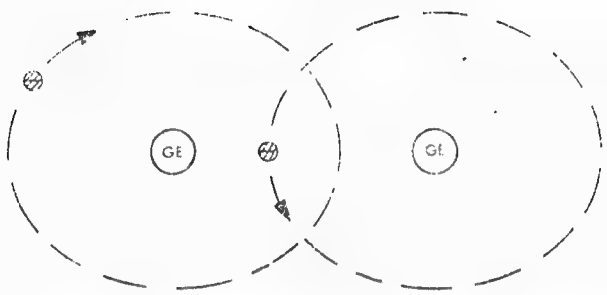


FIGURE 2.3 Configuration of Electrons

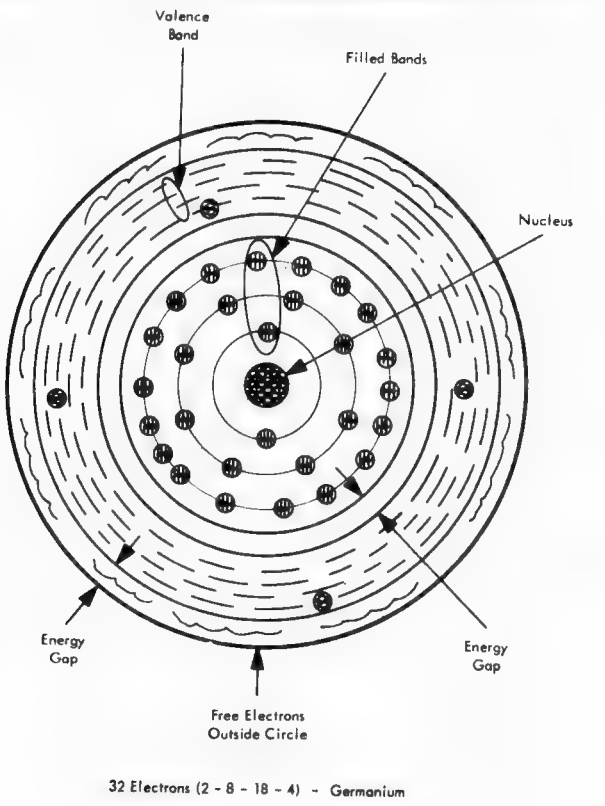


FIGURE 2.4 Germanium Atom

N-TYPE GERMANIUM

Intrinsic germanium is a relatively poor conductor. If controlled amounts of impurities are added, more current can flow. Adding impurities to intrinsic germanium is called doping. Antimony is an impurity used for this purpose. It has filled bands of 2, 8, 18, and 5 electrons are in the outer or valence band, Figure 2.6. Antimony has one more electron in the valence band than germanium has. This additional electron, comparing antimony to germanium, can be easily removed from the valence band. Four of antimony's valence electrons combine in the co-valent banding effect with other germanium atoms. Since it is much easier to remove an electron in a valence band that is not co-volent bonded, the fifth electron of antimony allows conduction in the doped material to take place with relative ease. It is said that this excess electron is donated to the conduction band. When an electron is given up by an atom, it is lost into free space or the conduction band. N-type germanium is so named because the majority current

N-Type Germanium (continued)

carriers are electrons, and since the electron has a negative charge, hence the name N-type germanium.

At normal room temperature, the donor electrons, as well as a few from the co-valent banded groups, are thermally agitated out of the valence band. These electrons that have escaped into the conduction band are now free current carriers. At normal room temperatures, N-type germanium always has a supply of electrons available for conduction.

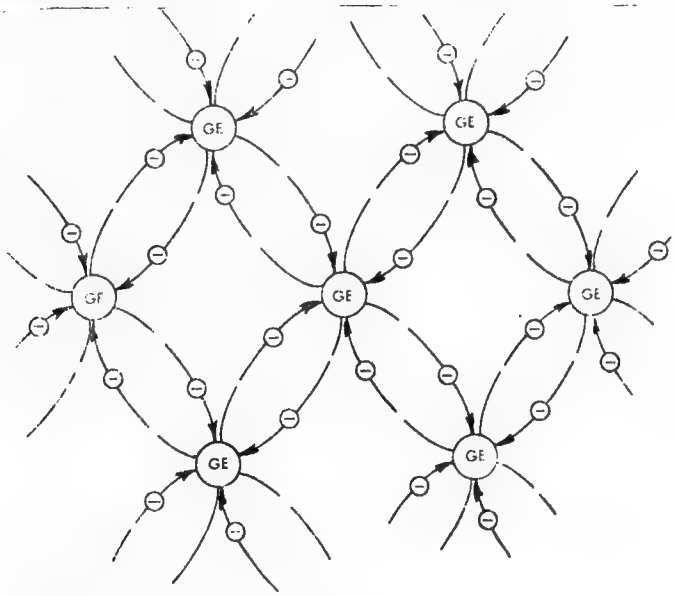


FIGURE 2.5 Diamond-Shaped Lattice Network of Germanium Atoms

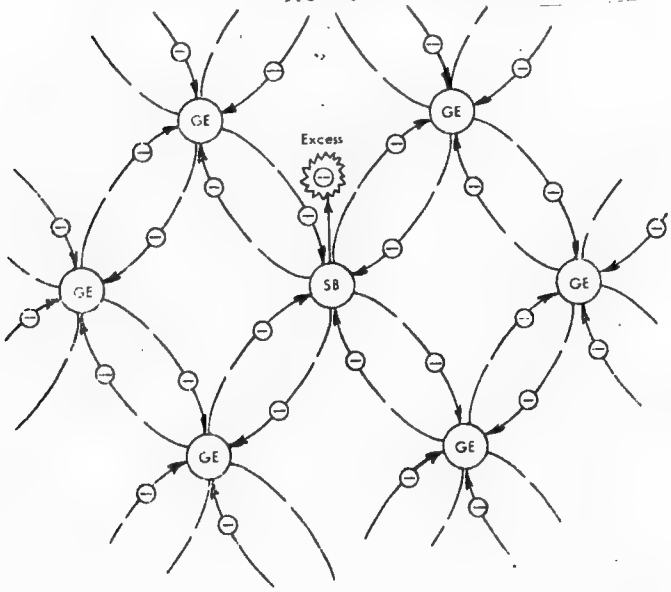


FIGURE 2.6 Lattice Network of N-Type Germanium

N-Type Germanium (continued)

When an electron escapes into the conduction band, it leaves behind an atom that now has a positive charge because it has lost one electron. The impurity atom that lost the electron cannot move about because it is held in position by the diamond shaped lattice network and is said to be a bound positive charge.

In the above discussion, heat (normal room temperature) was used to free electrons for the conduction band. Other external means may also be used to break valence electrons loose for the conduction band. A small voltage may be applied across a piece of N-type germanium which will cause a reasonably large amount of current flow. This current is a function of the number of donor electrons available in the material and is called extrinsic conductivity.

P-Type Germanium

Germanium can also be doped with other materials, such as indium. Indium has 3 electrons in the valence band. When germanium has been doped with indium, the indium atom has the equivalent of 7 electrons in a valence ring, 3 of its own, and the effects of 4 electrons from the adjacent germanium atoms, Figure 2.7. This leaves a position for a valence electron which would be needed to fulfill the octet theory. With this open position available, the indium atom is ready to accept an electron from any source. For this reason, the impurity indium atom is called an acceptor atom. If an electron from an outside source fills this position, the atom has gained one negative charge. Since the atom is not free to move about in the diamond lattice network, the atom is locked in place in the crystal and the electron is tightly held in the structure by co-valent banding. The indium atom is then known in a bound negative charge. When a doped piece of germanium has been made with indium atoms, there is enough thermo activity at room temperatures to keep the acceptor positions filled, leaving vacancies in the valence band of germanium atoms equal to the number of acceptor impurity atoms present in the crystal. These open position for electrons are known as holes. So at normal room temperatures there is a constant supply of holes available in the P-type germanium. Therefore, in P-type material, movement of holes is a form of current flow. In P-type germanium, holes are the majority current carriers.

P-Type Germanium (continued)

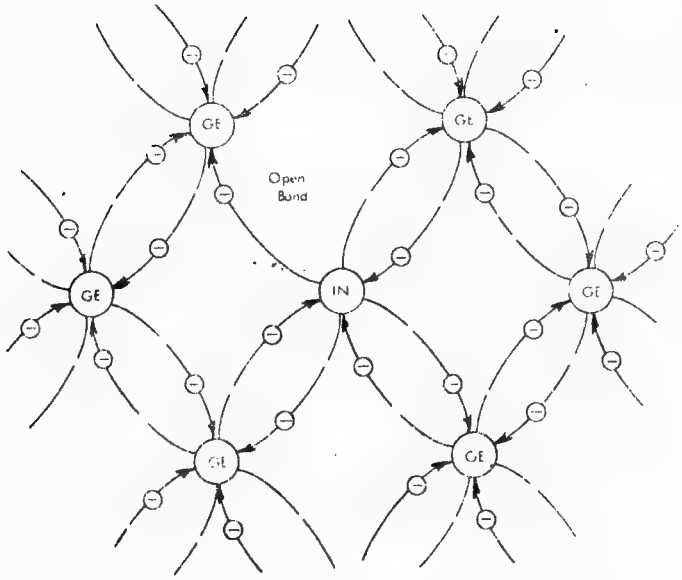


FIGURE 2.7 P-Type Germanium

If a small voltage is placed across a piece of P-type germanium, the holes will migrate toward the negative terminal. Actually, electrons will move from the valence band of one atom to the valence band of the next, without requiring the additional energy needed to jump into the conduction band. This effect is called hole current flow.

Intrinsic Conduction

In intrinsic or pure germanium, current carriers also exist. At normal room temperatures, co-valent bands are broken at random by thermo agitation. When a co-valent band is broken, an electron is freed, and a hole is left behind. It should be understood that the number of electrons and the number of holes must be equal at all times. Intrinsic conduction is the sum of the two components, part of the current being carried by the electrons, and part by the holes.

In doped germanium, either P or N type, intrinsic conduction also takes place. In P-type germanium, although holes are

Intrinsic Conduction (continued)

created by doping, a portion of conduction is caused by electrons. Of course, the holes far outnumber the electrons, and since this is the case, the holes are majority carriers. Since intrinsic conduction can also take place in P-type germanium, electron flow caused by this process is considerably less. Therefore, electrons contribute only a small fraction of the over-all current and they are called minority carriers. Conversely, in N-type germanium, intrinsic conduction also occurs, and a movement of electrons and holes in the valence band contribute to a small portion of the current flow. Therefore, in N-type germanium, the hole is the minority current carrier.

In summary, the following conclusions can be drawn. In N-type germanium, majority current (electron) flows in the conduction band, while minority current (hole) flows in the valence band. In P-type germanium, hole current (majority current) flows in the valence band, and electron current (minority) flows in the conduction band. One additional fact should also be recognized, that is that an electron has a greater mobility in the conduction band (it being free) than the hole does in the valence band.

When intrinsic conduction occurs, that is an electron is driven into the conduction band, leaving behind a hole, it is said that a couple has been formed, or an electron hole-pair has been formed. As the temperature of a piece of doped germanium is raised, more couples are formed, and the ratio of majority to minority carriers decreases. At extreme elevated temperatures, the ratio approaches 1 to 1 and the extrinsic identify of the doped piece of germanium is lost, and becomes essentially intrinsic.

DIODE THEORY

P-N Junction Barrier

When N and P-type germanium are fused together, so that an atomic bond exists between the two materials, a rectifying action takes place at the junction. If an understanding of this phenomena is understood, the majority of the principles of transistor action will have already been learned. In Figure 2.8 a piece of N-type

P-N Junction Barrier (continued.)

germanium and P-type germanium have been atomically bonded together. The minus signs shown in the N material show that there are free electrons available. Also in the N material, the plus signs drawn inside a shaded circle, are bound positive charges. In the P material, the plus signs are holes, and the minus sign inside the shaded circles are bound negative charges.

At normal room temperatures, the majority of the donor atoms have lost their electron and can be considered to be distributed uniformly throughout the material. Each donor atom that gave up its 5th electron, becomes a bound positive charge. A donor electron that has escaped into the conduction band is moving about in a random fashion. Even though electrons are moving about within the material, a neutral charge situation exists overall within the material.

A similar condition also exists in the P region. At normal room temperatures, the majority of the acceptor atoms have received electrons from their adjoining germanium atoms. Atoms that have lost an electron, the electron having been received by an impurity atom, provide a random movement of hole current flow throughout the material.

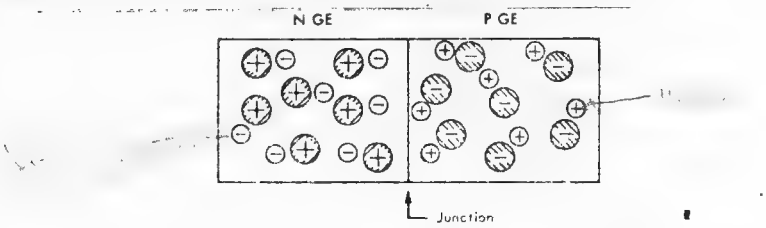


FIGURE 2.8 N-P Junction

An electron in the N material that is close to the junction can move across the junction into the P material. Conversely, a hole in the P material that is near the junction can also move into the N region. Figure 2.9 shows the random movement of electrons and holes crossing the junction. When a free electron from the N region moves across the junction into the P region, it will re-combine with a hole that is close to the junction. Each electron has left behind a bound positively charged atom. When a hole crosses the junction into the N region, an electron from the N region will re-combine with it and eliminate the hole. Each hole that has crossed the

P-N Junction Barrier (continued)

junction, has left behind a negatively bound charge. The random crossing of electrons and holes across the junction, which leaves behind bound positive and negative charges, is primarily concentrated in the area close to the junction. Therefore, in the N region, an area within the material becomes significantly positively charged, while in the P region, the bound negative charges close to the junction area exhibit a concentration of negative charges. Thus, the N side has fewer free electrons to balance the bound positive charges near the junction, and P side has fewer holes available to balance the bound negative charges near the junction.

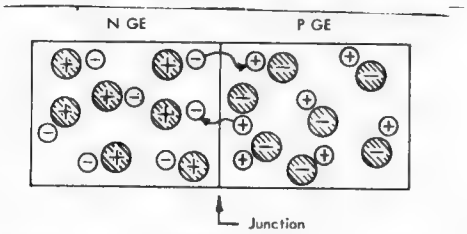


FIGURE 2.9 Formation of N-P Junction

This results in a build-up of an electro-static charge on each charge on each side of the junction. Figure 2.10 shows an N-P junction after the majority of random crossings has occurred. The region about the junction that has all bound charges is called the depletion region. This means that there are no majority current carriers within the depletion region. Actually, the junction area is not well defined as shown in Figure 2.9, but extends from the junction out into both areas in a decreasing manner. Figure 2.11 shows a graph of the electro-static charge from one end of the N material to the other end of the P material. When considering this piece of N-P material at normal room temperatures, there is the continual formation of electron-hole pairs. The electro-static charge of the junction, therefore, continues to vary at an average rate.

P-N Junction Barrier (continued)

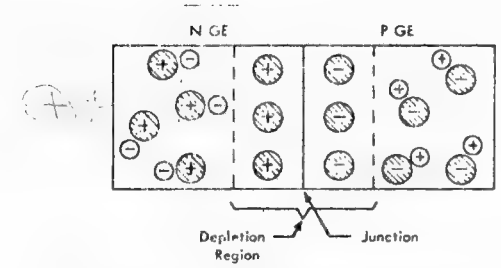


FIGURE 2.10 Depletion Region Formed

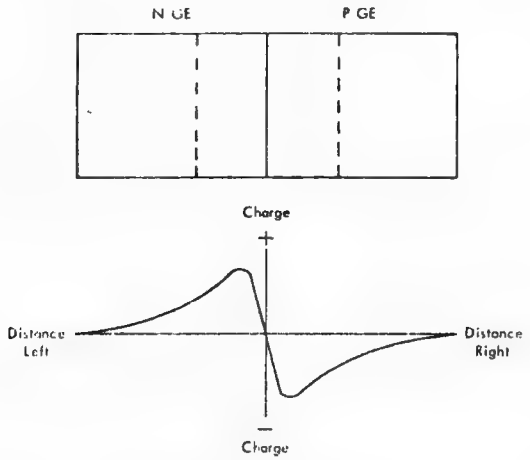


FIGURE 2.11 Charge Distribution of an N-P Junction

Reverse Biased N-P Junction

When a battery is applied to the N-P junction with the positive terminal connected to the N region and the negative terminal connected to the P region, the junction is said to be reverse biased, Figure 2.12. The positive terminal of the battery can attract free electrons from the N region, and the negative terminal of the battery can attract holes in the P region. With the majority carriers moving away from the depletion region, more bound charges appear in the material.

Since the battery is a source of electrons, it will provide electrons and deliver them to the P region. Also, it will

Reverse Biased N-P Junction (continued)

remove an equal number of electrons from the N region and in so doing, produce current flow in the external circuit. The battery is capable of supplying an electron to the P region only after it has been capable of extracting an electron from the N region. The current that flows in the external circuit due to this process is the reverse biased current.

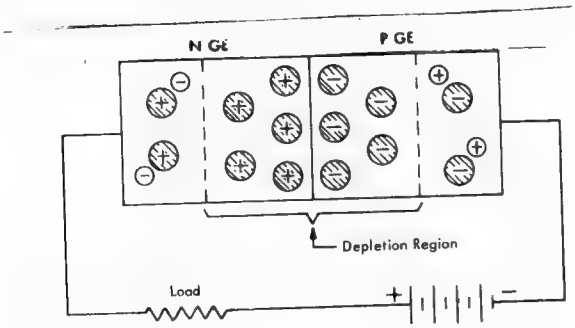


FIGURE 2.12 Reverse Biased N-P Junction

Just prior to the connection of the battery across the N-P junction, there were free carriers available at the terminal ends of the junction. The moment the battery was connected, the number of bound charges in the material increased. When the number of bound charges increases, the number of free carriers that are available decreases. Therefore, very soon after the battery has been connected in a reverse manner across an N-P junction, the supply of free carriers in the material decreases, and consequently, the amount of current that can flow in the external circuit is limited.

The action described above, has been primarily associated with the current carriers made available as a result of doping the germanium. Free carriers can also be created near the junction by imparting additional energy to the material. At normal room temperatures, electron hole pairs occur. If an electron hole pair is generated in the P region, the free electron, a minority carrier moving at random, may reach the junction during its life time. It is attracted across the junction toward the N region by both the carrier and the external bias applied. If the electron does cross into the N region, the N region contains 1 additional electron, and the P region 1 additional hole. Therefore, the N region has

Reverse Biased N-P Junction (continued)

a free electron that can be delivered to the positive terminal of the battery, and the P region can accept an electron from the battery, filling the hole.

A similar process can occur if the electron hole pair occurs in the N region. If the minority carrier, being the hole in the N region, reaches the carrier, it can be attracted across the junction by the bound negative charges in the P region and the external bias applied from the battery. The hole originally supplied from the N region, crossing the junction into the P region, now becomes a majority carrier and will proceed toward the negative terminal.

Since electron hole-pairs are generated at normal room temperatures and will supply current carriers within the material that also provides current flow in the external circuit, the reverse current that flows in the external circuit is intrinsic because of the generation of minority carriers. Not all of the minority carriers that are generated at normal room temperatures will cross the junction, but will re-combine. Those carriers that are produced and reach the junction, depend somewhat on the bias supply, but to a larger extent on the minority carrier lifetime, which is a function of the density of majority carriers or the amount of doping. It is also evident from this discussion that if the reverse bias current is stabilized at a given temperature, then when the temperature is increased, the number of minority carriers generated will also increase, thus supplying a larger amount of carriers for an increased amount of reverse biased current.

As the reverse biased battery potential is increased, there is only a slight increase in the reverse current up to a given point, then a rapid increase limited only by the amount of resistance in the external circuit. Normally the amount of reverse current that flows when a N-P junction is reverse biased, is very small. Therefore, under these circumstances, the N-P junction exhibits a very, very high resistance to the external circuit.

Figure 2.13 shows the symbols for the reverse biased N-P junction and the characteristic curve. When the reverse biased current increases very rapidly with only a small change in bias

Reverse Biased N-P Junction (continued)

potential, the junction is said to have reached breakdown and the reverse resistance of the junction decreases rapidly. There are two types of situations which will cause N-P junction breakdown. They are discussed in the two following paragraphs.

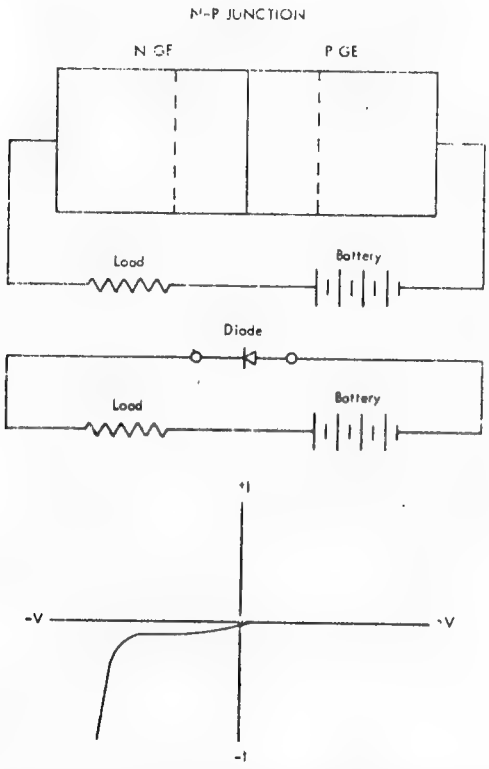


FIGURE 2.13 Characteristic Curve of Reverse Biased N-P Junction

Avalanche Breakdown

When electrons come under the influence of an electric field, they gain energy. As the reverse biased potential is increased, the minority carriers that cross the junction are accelerated and acquire sufficient energy to bombard and dislodge valence band electrons from the germanium atoms. This increases the number of electrons available in the N region that can be supplied to the external circuit. Holes

Avalanche Breakdown (continued)

that are developed in the N region can cross the junction and repeat this process in the P region. When sufficient bias voltage is supplied to start the avalanche breakdown action, that of generating electron hole-pairs, the external reverse bias current increases rapidly. If the resistance in the external circuit does not limit this current, then the heat generated within the N-P junction can very quickly destroy the device.

Zener Breakdown

The force in an electric field exerted on an electron is proportional to a strength of the field, and is measured in volts per centimeter. The voltage that appears across the junction of an N-P device is small, but it is concentrated in such a short distance that fields can exist with a magnitude of 100,000 volts per centimeter or more. When this electric field becomes sufficiently strong, valence bonded electrons are pulled from their orbits and provide a source of current carriers. If zener breakdown is compared with avalanche breakdown, it becomes evident that avalanche breakdown is a current multiplication process that can be compared to secondary emission in a vacuum tube. Zener breakdown, on the other hand, can be described as a condition that results from the application of an electric field. This breakdown is unique and stable for each particular diode and finds many useful applications as a voltage reference.

For each case of breakdown, the amount of reverse current is limited by the resistance of the external circuit and not by the junction itself. The breakdown currents do not damage the junction unless the power dissipation is increased to a point where the temperature rise causes physical damage to the junction. The power rating of the junction is equal to the product of the voltage across the junction after breakdown, and the current flowing. The power rating of these units ranges from a few milli-watts to well over several watts. The power dissipation rating can be increased by the use of a dissipating surface, commonly called a heat sink.

Forward Biased N-P Junction

When a battery has its positive terminal connected to the P region and the negative terminal connected to the N region, Figure 2.14, the junction is forward biased. The battery potentials connected in the forward biased manner, repel the majority carriers of each region, toward the junction. This causes free electrons in the N material to re-combine with the bound positive charges near the barrier. The majority carriers in the P region are driven toward the junction and re-combine with the bound negative charges. This reduces the electro-static charge at the junction and depletes the depletion region.

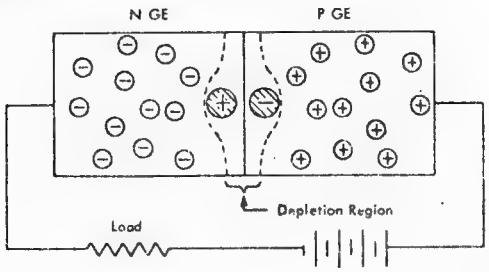


FIGURE 2.14 Forward Biased N-P Junction

Majority carriers that do not re-combine, diffuse through the barrier and become minority carriers on the opposite side. The majority carriers that pass through the junction and become minority current carriers appear at the terminals and constitute external circuit flow.

The high velocity of the minority carrier electrons causes them to dislodge other valence electrons in the P material, so that more carriers are added to the conduction process. The charge of the minority carrier electrons also develops an electric field that further assists the transfer of thermally generated majority carriers toward the junction. This process is accumulative and results in a flow of carriers that greatly exceeds the amount that would normally be governed by the resistivity of germanium.

Since the barrier is depleted at the junction when forward bias voltage is applied, the resistance across the junction is reduced nearly to zero. There is a small voltage drop

Forward Biased N-P Junction (continued)

at the barrier and also a small amount is dropped in both the N and P regions because of the inherent resistivity of the material. Therefore, the N-P junction appears as an extremely low resistance to the external circuit when it is in a forward bias state. Figure 2.15 shows the symbols for the reverse biased junction and the forward portion of the characteristic curve. The resistance of the external circuit is the only current limiting device, and the value of the external resistance must be so selected that the heat dissipation rating of the junction not be exceeded. The majority of N-P junction devices have only a few tenths of a volt drop across them when they are in the forward conducting direction.

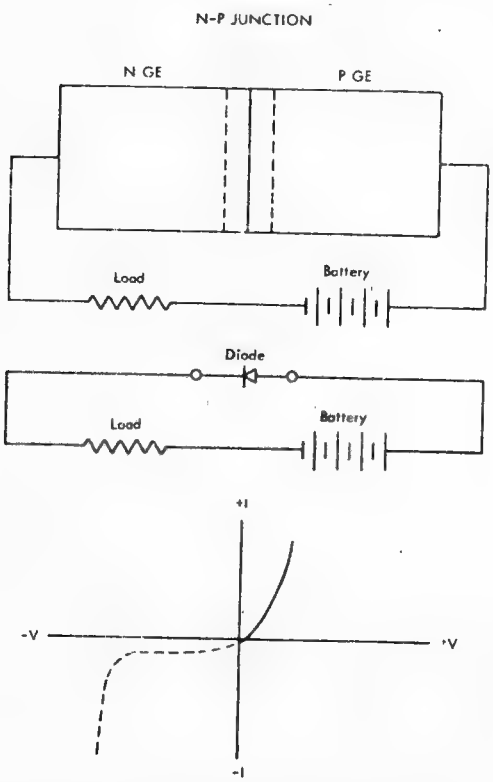


FIGURE 2.15 Characteristic Curve of Forward Biased N-P Junction

SIGNED ASSYNCHRONOUS BINARY ADDER

CHAPTER 3

TRANSISTOR THEORY

CHAPTER 3.

TRANSISTOR THEORY

Alloyed-Junction Construction

The construction of a typical PNP alloyed or fused junction transistor is shown in Figure 3.1A. An N-type germanium block about .002 inch thick and .060 inch square is used for the base material. An indium dot .010 inch in diameter is used for the emitter. A slightly larger indium dot, .020 inch, is used for the collector. Each of these dots is alloyed to the base by controlled heating, the resulting crystal has an P-type impurity layer at each of the two junctions. The depth of penetration of the P-type layers into the base is dependent upon the time and temperature of the alloying process. This penetration determines the final thickness of the base which will be about .0003" This dimension is extremely critical and one of the problems complicating the manufacture of uniform transistors.

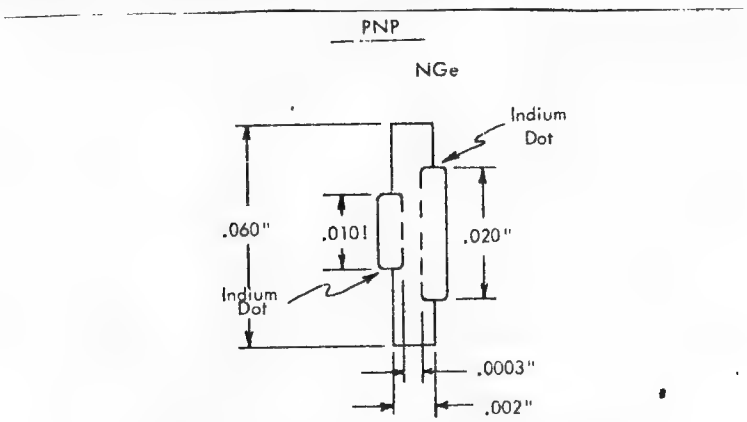


FIGURE 3.1A Transistor Dimensions

A gold plated ring is bonded to the base material; wire leads are then fused to the gold ring and to the emitter and collector dots. The assembly is mounted on a glass base and the entire unit is hermetically sealed in a small metal container, Figure 3.1B&C.

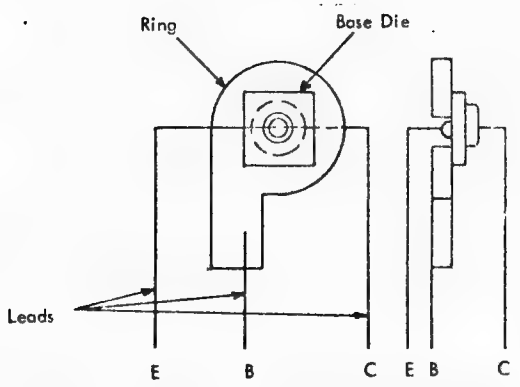


FIGURE 3.1B Transistor Arrangement

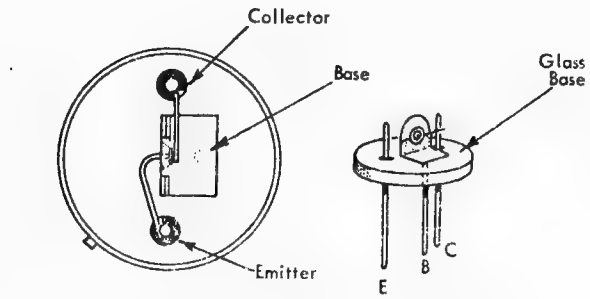


FIGURE 3.1C Transistor Packaging

In order to conform to an industry standard and allow automated card assembly, the packaging is shown in Figure 3.1D. In this case, looking at the bottom of the unit and starting at the tab, the leads are emitter, base, and collector, reading in a clockwise direction. The tab is used to provide physical orientation for assembly on the SMS card.

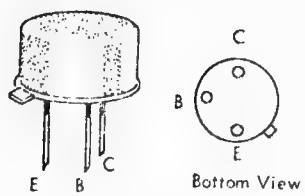


FIGURE 3.1D Transistor Encasement

The IBM schematic symbols are shown in Figure 3.1E&F. The arrow always identifies the emitter and also by its direction, whether the transistor is a PNP or an NPN device. If an NPN transistor were shown in Figure 3.1A, then the base die would be made from PGe and Antimony dots used for the emitter and collector.

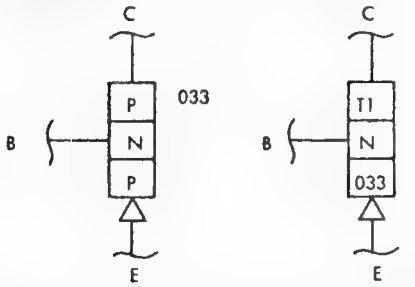


FIGURE 3.1E PNP Transistor Symbols

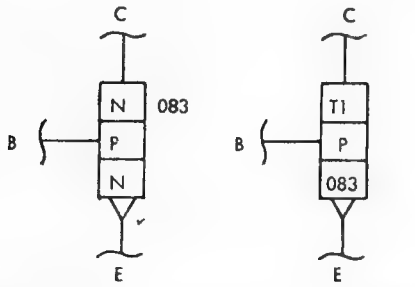


FIGURE 3.1F NPN Transistor Symbols

Static Condition

When the crystal is formed, the majority carriers cross the two junctions exactly in the same way as in a diode, forming two depletion regions, Figure 3.2. This condition exists before any external potentials are applied.

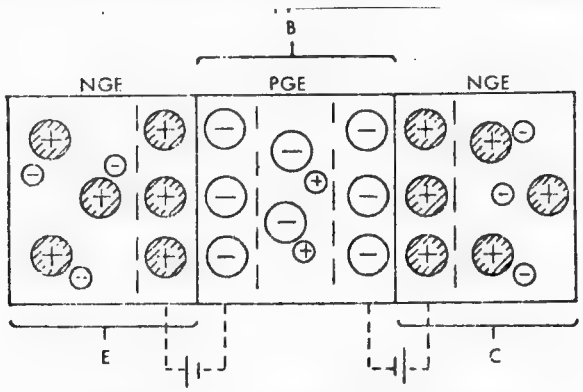


FIGURE 3.2 Transistor Junctions

Reverse Bias

Figure 3.3 shows a reverse-biased NPN transistor and the current flow that exists. The E-to-B diode and the C-to-B diode are both reverse biased because the battery polarity connects to unlike elements. Reverse current flows from base to emitter and base to collector. The B-to-E current is called I_{ebo} for current flow, emitter to base, with the collector open-circuited. The B-to-C current is called I_{cbo} for current flow, collector to base, with the emitter open circuited. I_{ebo} and I_{cbo} are generally used in the reduced form of I_{eo} and I_{co}. I_{co} and I_{eo} are small currents in the order of 2-60 μa for high-frequency transistors. Although this current may seem small, I_{co} is an important consideration in circuit design because it flows in the output circuit, which is generally a high impedance.

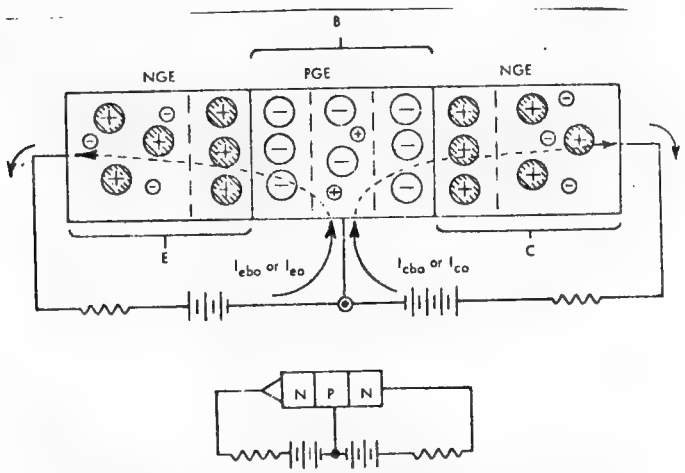


FIGURE 3.3 Reverse Biased Transistor

Forward Bias

The NPN transistorcircuit of Figure 3.4 is forward biased and is identical to Figure 3.3 except that the E-t o-B battery is reversed. Forward bias drives majority carriers to the barrier region in abundance. Majority carriers reduce the depletion region to zero, and in addition set up a barrier potential which "aids" majority carriers across the barrier.

Forward Bias (continued)

It is obvious that electrons are attracted into the base region and holes are attracted into the emitter region.

General Operation of a Transistor

Basically, an external circuit controls the emitter-to-base bias, which in turn controls current flow from the emitter to the collector. Bias control works as follows:

Emitter to Base

1. reverse bias prevents current flow from the emitter to collector.

2. forward bias permits emitter-to-collector current flow.

3. the degree of emitter to base forward bias controls the amount of emitter-to-collector current.

4. the collector-to-base is always reverse-biased for transistor action.

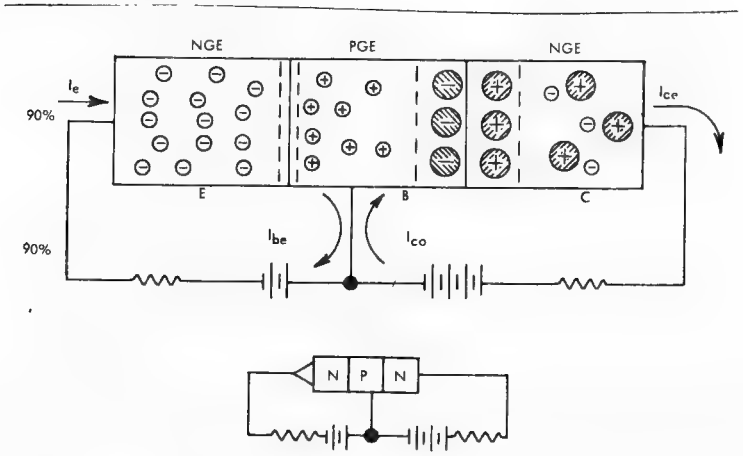


FIGURE 3.4 Forward Biased Transistor

Although transistors do not act identically to tubes, certain similarities exist. For instance, in tube circuits, a signal is fed to the grid or cathode to control current through the tube, and in a transistorcircuit a signal is fed to the base or emitter to control current through the transistor, Figure 3.5

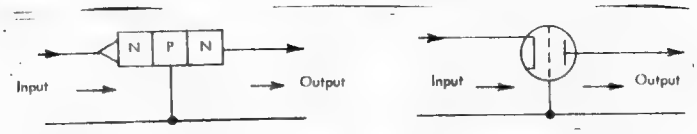


FIGURE 3.5A Common Base Transistor-Common Grid Tube Circuits

In Figure 3.5.A the input signal is applied to the emitter of the transistor with the base common to both input and output. The tube counterpart has the input signal applied to the cathode. A tube connected in this manner is called a grounded grid stage and the transistor arrangement is termed a grounded or common base configuration.

In Figure 3.5B, the common element is the emitter and cathode. This arrangement is referred to as the common emitter and grounded cathode respectively. The input signal is applied to the base and grid. The characteristics are as follows:

1. Low input impedance
2. Fairly high output impedance
3. High Voltage Gain
4. High Current Gain
5. High Power Gain
6. The output signal is 180^{o} out of phase with the input signal
7. Most widely used circuit configuration.

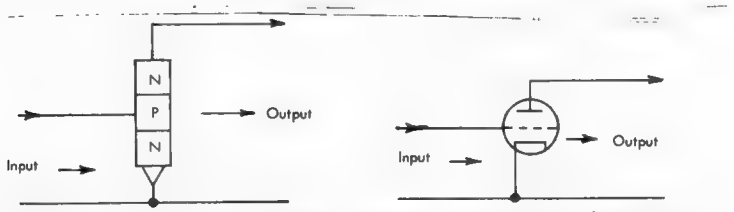


FIGURE 3.5B Common Emitter Transistor-Common Cathode Tube Circuits

The circuit capabilities between the tube and transistor circuit are similar. In this configuration, the following characteristics are:

1. Low Input Impedance
2. High Output Impedance
3. Is used for an impedance matching device
4. Extremely High Voltage Gain
5. The Current Gain is less than one
6. The output signal is in phase with the input signal.

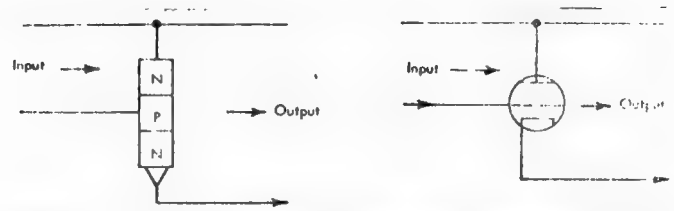


FIGURE 3.5C Common Collector Transistor-Common Plate Tube Circuits

The last circuit configuration is the common collector and common plate. The output is taken from the emitter and cathode respectively. These circuits are more commonly referred to as the emitter follower and cathode follower. Characteristics are as follows: (Figure 3.5C).

1. High Input Impedance
2. Low Output Impedance
3. Is used for an impedance matching device
4. Extremely high current gain
5. The voltage gain is less than one
6. The output signal is in phase with the input signal.

Further analysis of a transistor' s electrical characteristics will be clear, if its physical properties are again studied. Remember that the emitter junction has a large surface area (compared to the base width) and the collector junction has an even larger surface area. These two large surface areas are extremely close to one another. This is similar to two capacitor plates spaced close together. With this in mind, study Figure 3.6, which is a cross-sectional view of an NPN transistor. The outer areas containing the NGe are considered as part of the external circuit; i.e., they contain the non-alloyed bulk of the emitter and collector dots and their ohmic value is practically zero. The actual emitter is the alloyed region shown containing an electron source. The actual collector is the alloyed region shown, similar to the emitter region except that it is larger. The base, of course, is the region between the emitter and the collector which is drawn as a rectangle containing "holes".

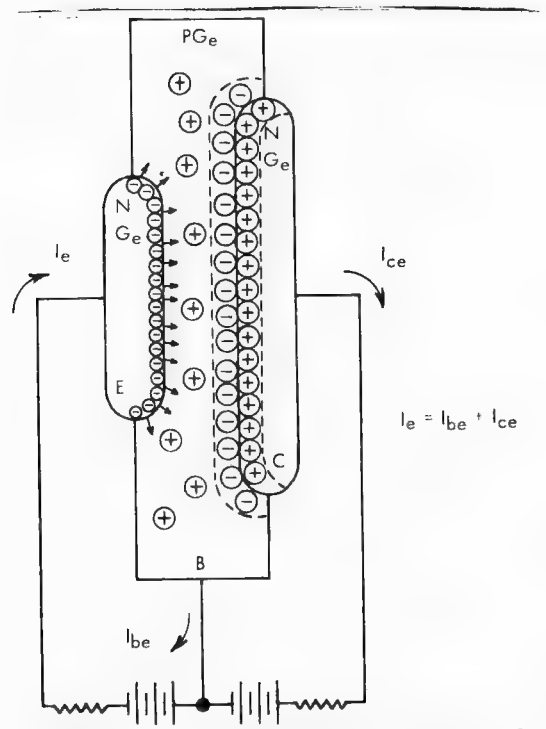


FIGURE 3.6 Cross-Sectional View of an NPN Transistor

Again study Figure 3.6, only this time try to picture what happens electrically while not forgetting what the physical properties are. This study should reveal the following:

1. The emitter-to-base junction is forward biased.
2. The collector-to-base junction is reverse biased as it always is in transistor circuits.
3. Current entering the emitter is called I_e.
4. I_e flows into the base region where it divides into I_{be} (base-to-emitter current) and I_{ce} (collector-to-emitter current).
5. Electrons entering the base find the most direct route to a positive potential by travelling to the collector region.
6. Because the collector is larger than the emitter, many of the electrons leaving the periphery of the emitter still reach the collector.

General Operation of a Transistor (continued)

7. Most base current occurs because electrons emitted from the emitter periphery are not directed toward the collector. (See the emitter geometry). These electrons find the base potential a more direct return than the collector potential.

Minority Carriers

Because the whole concept of transistor action deals with pushing minority carriers into the base and then acting on these carriers, this action will be more closely investigated.

Most minority carriers reach the collector. This is so because the collector is made larger than the emitter and is spaced very close to it (approximately .0003" to .0006"). Therefore, very few emitted carriers can escape this direct path to the collector region. Nevertheless, some do. Some carriers do not reach the collector primarily because of the geometry of the emitter periphery. Carriers leaving the emitter periphery enter the base at angles almost perpendicular to the emitter surface, which is not perpendicular to the collector plane. Therefore, these carriers can migrate to either the collector region or the base surface.

Many people find it helpful to compare transistor operation to tube operation. In some areas the operation is similar while in others it is not. Of course, it is mostly the "not" areas that require explanation. Minority carrier flow through the base is a "not" area; that is, this action is not similar to current flow in a tube. Current flow in a tube, you recall, requires the emitting element (cathode or filament) to emit free electrons into a vacuum, after which the potentials of the grid and plate act on these electrons. The point here is that in tubes the free electrons move from one point to another, because of the attraction or repulsion of a potential acting on them. This is not true of minority carrier current in the base.

Minority carriers entering the base are not influenced by a potential, because none exists in the base region; the base region is a neutral region. Of course, the base-to-emitter and base-to-collector barriers exist, but only at the junction regions, and they do not extend any appreciable distance in to the base region.

Diffusion Current

If potentials are not acting on minority carriers in the base, what is? Diffusion is. Diffusion results whenever like charges collect. Like charges repel, so they try to get away from one another. This "getting away" is a spreading out or diffusion process.

Actually, diffusion is only part of the picture. The other part is the path taken by a minority carrier while travelling to the collector. The ideal path would, of course, be straight across, but a minority carrier may instead follow a random path as shown in Figure 3.7. A random path results when a minority carrier comes under the influence of charges in the base; that is, the minority carrier is deflected by a collision with an atom or by a concentration of charges existing in a location it is entering.

It may appear that diffusion current is a rather haphazard action, that minority carriers "float" over to the collector. Actually this is not so. Diffusion current also has a direction and force component because of emitter action; the emitter is continuing to supply the base with minority carriers which force those previously emitted away from the emitter. this action causes a diffusion gradient to exist in the base as shown in Figure 3.8

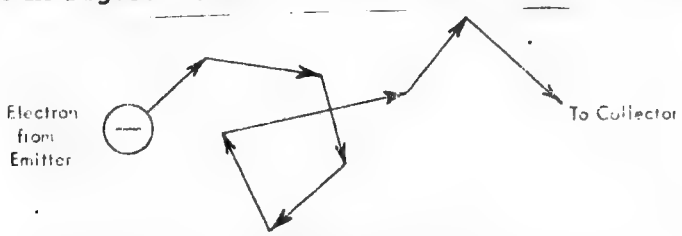


FIGURE 3.7 Random Path of Minority Carrier in Base Region

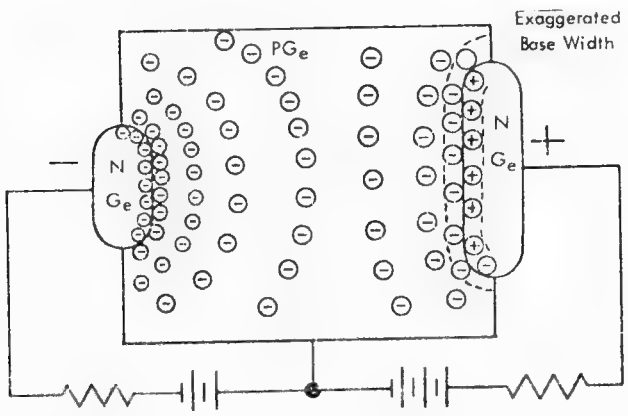


FIGURE 3.8 Diffusion Gradient in Base Region

Current Sinks

Minority carrier transit in the base is shown in Figure 3.8. Because a clear understanding of this action will be helpful later, take the time to study this drawing carefully. See how a high concentration of minority carriers exists at the emitter and how the concentration decreases as carriers approach the collector. Actually, minority carriers in the base are searching for a return to a source or "current sink". The collector, of course, is a good sink because minority carriers reaching the collector become majority carriers and are swept away through the collector region. The surface of the base region adjacent to the emitter is also a good sink because surface germanium atoms have incomplete covalent bonds. These surface atoms bond with atoms on three sides only and, therefore, each has a hole location. In other words, when the crystal surface is reached there are no more atoms and the lattice is no longer diamond shaped.

This surface structure makes the surface resistance of germanium much less than the resistance of the bulk material. For this reason, practically all base current originates when minority carriers reach the base surface adjacent to the emitter and recombine.

Base Recombination

Recombination is a difficult concept for many to understand clearly, so base surface recombination will be analyzed closely. The sequence of activity is as follows:

1. Hole locations exist on the surface because of the incomplete covalent bonding of germanium atoms.

2. The surface looks like a positive location to minority carrier electrons in the base.

3. Minority carriers reach the surface and recombine (attach themselves to germanium atom locations)

4. Once surface recombination takes place, the region has lost its neutrality and is acted on by the positive potential applied to the base.

5. Surface current flows to return the recombination region back to a neutral state.

Base Recombination (continued)

6. The amount of surface current that flows is determined by how rapidly charges can move across the surface.

7. A high surface velocity restores the recombination region back to normal fast; that is, it "cleans out" the base surface current sink rapidly so that the sink can again attract minority carriers.

8. The rate or recombination if proportional to surface velocity.

9. Surface velocity should be kept as low as possible so that base current is held to a minimum. We will find later that transistores having the best gain characteristics are those in which the percentage of minority carriers reaching the collector is high and the percentage reaching the base is low.

10. The surface is contaminated by gas atoms from the atmosphere joining into the surface structure. This contamination usually results in increased surface velocity and is not desirable. Therefore, the surface is chemically treated in the manufacturing process and the transistor is sealed for protection from the atmosphere. Broken seals reduce the lifetime of a transistor through surface contamination, so treat them carefully.

It should now be clear that surface recombination is a dominant factor determining base current. Bulk recombination (recombination other than surface) also exists, but the quantity is small and can be disregarded.

A close look at the emitter should also reveal that minority carriers from the periphery set up a sort of minority carrier cloud, which tends to focus toward the collector those carriers emitted from the inner emitter area.

Signal Distortion

In Figure 3.9 an input signal with the resulting output signal (inverted) are shown. The output signal is not a true representation of the input.

The following statements describe the various times labeled in Figure 3.9

t_r is the rise time of the input pulse and is the time which the amplitude of the leading edge is increasing from 10% to 90% of the maximum pulse amplitude.

t_f is the fall time of the input pulse and is the time which the amplitude of the lagging edge is decreasing from 90% to 10% of the maximum pulse amplitude.

t_d is the turn-on delay time which is the time interval from when the input signal has reached 10% of its maximum amplitude to when the output signal has reached 10% of its maximum amplitude.

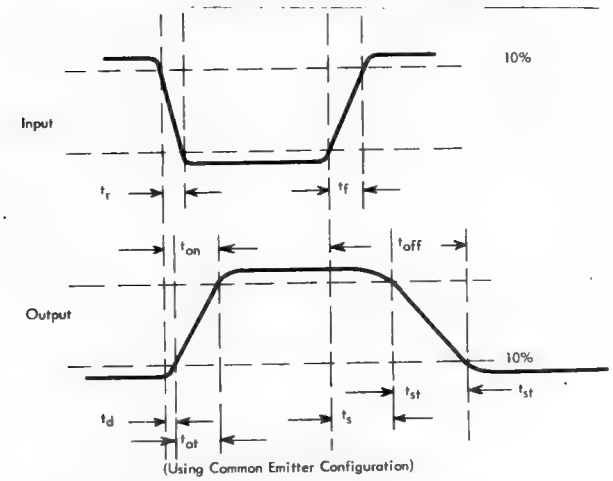


FIGURE 3.9 Distortion in Output Waveform

This delay results because carriers leaving the emitter become minority carriers which take a finite period of time to cross the base region. This time interval is called "transit time" The point of significance here is that even though the emitter is passing a signal, the collector circuit does not recognize this signal until emitted carriers reach the collector. When emitted carriers enter the collector region, others leave the collector region and flow through the external load. Think of this majority carrier current in the collector as you would a copper wire; for each carrier entering the collector, one leaves to enter the external circuit. Thus, current flow through the collector region does not delay the output signal.

t_{ot} is the turn-on transition time which is the time during which the current through the transistor is increasing from 10% to 90% of the maximum amplitude.

This phenomenon results because emitted carriers travel to the collector by random routes and because individual carriers travel through the base at different velocities. Therefore, all of the first carriers emitted do not arrive at the collector at the same time. Those that travel the most direct route at the fastest velocity arrive first, while those of slow speed which travel the least direct route arrive last. In any case, the non-uniform arrival rate means that the leading edge of the signal is distorted.

t_{on} is turn-on time and is the sum of turn-on delay and turn-on transition time of the output pulse.

t_s is the storage time (turn-off delay) which is the time interval from when the input signal has reached 90% of its maximum amplitude to when the output signal has reached 90% of its maximum amplitude.

It is due to transit time through the base. Thus, when the input signal is cut off, the output signal does not fall until the last increment of emitted carriers starts arriving at the collector.

t_{st} is the turn-off transition which is the time the current through the transistor is decreasing from 90% to 10% of its maximum amplitude. It is identical in nature to turn-on transition except that it takes place on the trailing edge of the signal.

toff is the turn-off time and is the sum of the turn-off delay time and the turn-off transition time of the output pulse.

Transistor Delay

In Figure 3.10, on NPN transistor is shown with an exaggerated Base Region with an accompanying time chart with a reverse bias potential applied.

At time t_1 the input is positive and the output is positive.

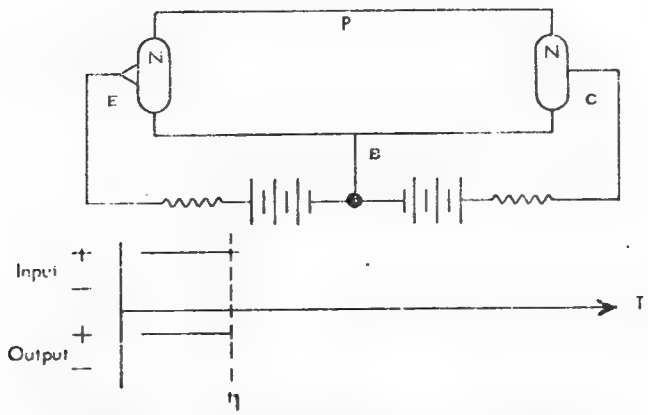


FIGURE 3.10A Transistor Delay-Time T_1

As the transistor is forward biased, Figure 3.10B, at Time t_2 the emitter starts emitting carriers in the base, however, the output sees no change.

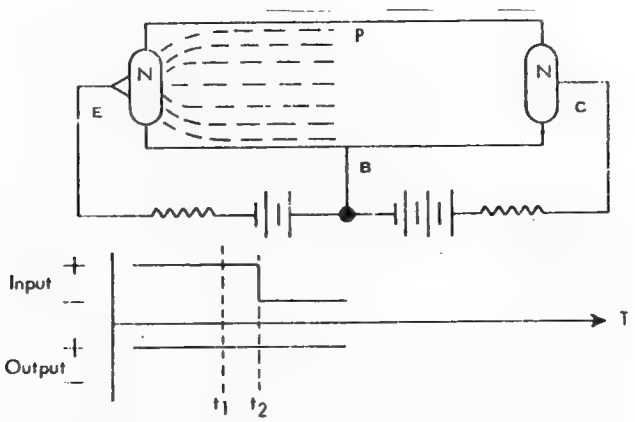


FIGURE 3.10B Transistor Delay-Time T_2

Transistor Delay (continued)

When sufficient time has passed for a few carriers to diffuse through the base, the output starts changing, Figure 3.10C at Time t_3.

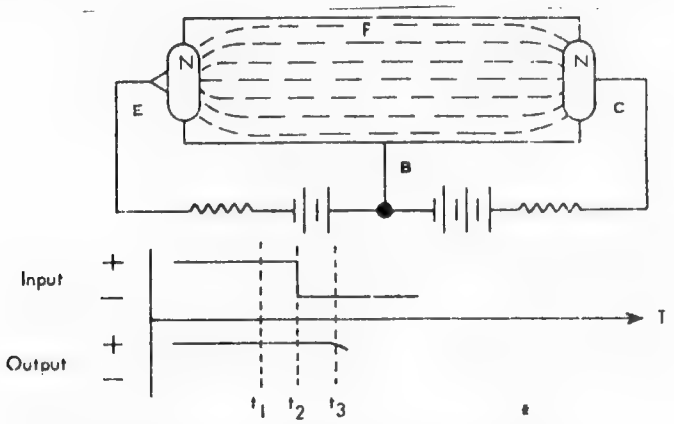


FIGURE 3.10C Transistor Delay-Time T_3

When the arrival rate of the carriers through the base region reaches a maximum average arrival rate the transistor, being forward biased, now has the original change of the input signal appearing at the output, Figure 3.10D, at Time t_4.

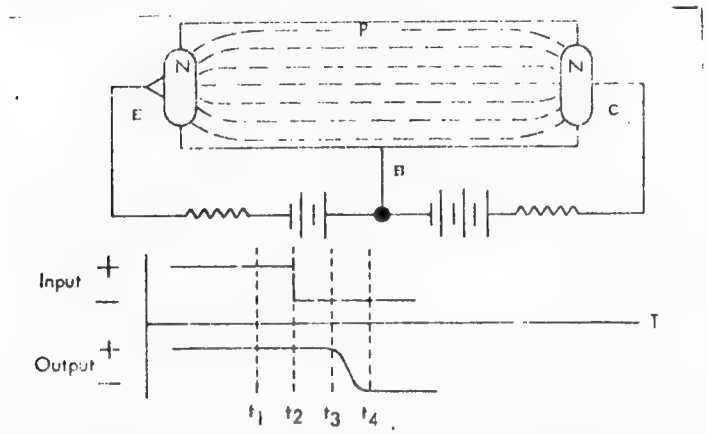


FIGURE 3.10D Transistor Delay-Time T_4

When the input signal is returned to its original level, the current carriers are still arriving at the collector at the maximum arrival rate and no change in the output is felt, Figure 3.10E, at Time t_5.

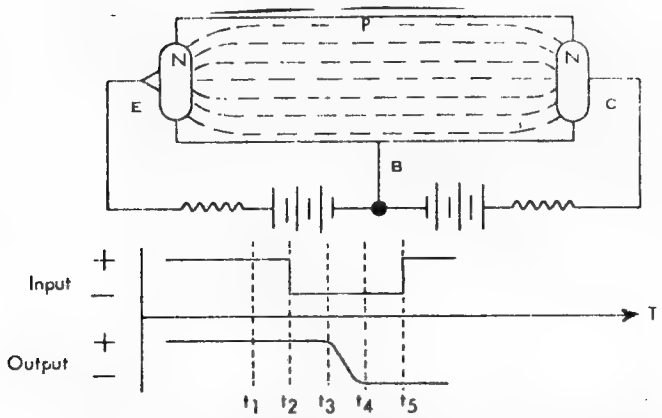


FIGURE 3.10E Transistor Delay-Time T_5

As the arrival rate of the carriers begins decreasing the change that occurred in the input at Time t_5 will start being felt at Time t_6, Figure 3.10F.

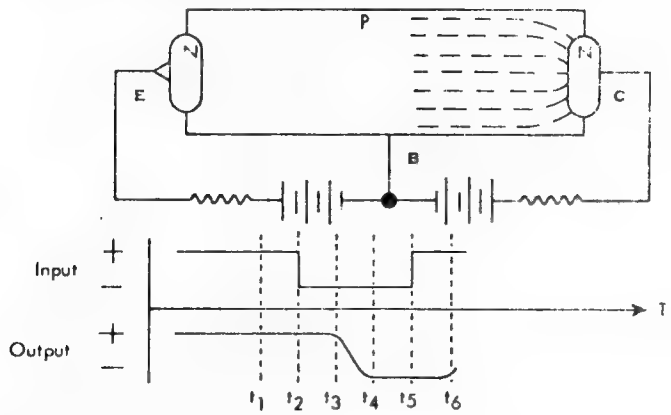


FIGURE 3.10F Transistor Delay-Time T_6

Finally as the last few carriers that are able to reach the collector, Time t_7 arrive, the output signal now has completely followed the input signal with both delay and distortion present, Figure 3.10G.

Transistor Delay (continued)

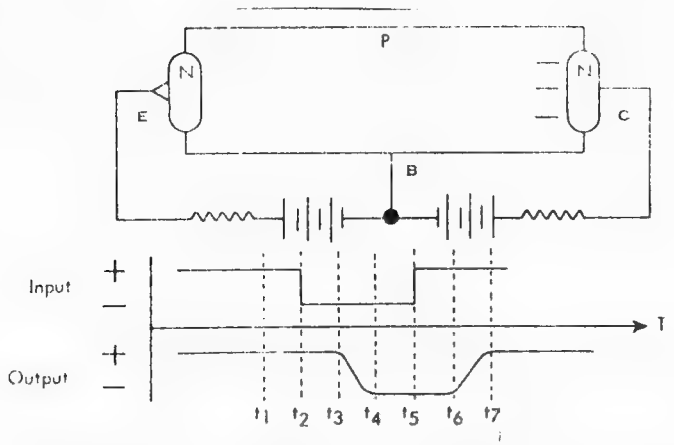


FIGURE **3.10G** Transistor Delay-Time T_7

Although transit time through the base is the major factor of turn-on delay, the base-to-emitter capacitance is also a contributing factor. This capacitance effect is explained as follows:

1. When the input signal has the base-emitter junction reversed biased, the B-to-E barrier is charged to the value of reverse bias and a depletion region exists.

2. When the input signal forward biases the base emitter junction, the majority carriers first fill the depletion region (a charge effect). After the depletion region is reduced to zero, majority carriers enter the base. Thus, the time required to reduce the depletion region to zero is part of turn-on delay.

3. Turn off delay is also affected by the external circuit load.

Frequency Response

Frequency response or distortion is an important transistor parameter because it establishes the highest pulse frequency that can be used effectively in a circuit (Figure 3.11).

Frequency Response (continued)

To show the effect of frequency response, a square-wave emitter signal of frequency f, f_1, f_2 and f_3 is used and the output signal is studied (Figure 3.11). Analysis of the output signal shows that:

1. At a low frequency f the output signal is an image of the input (no distortion exists).

2. At frequency f_1 (which is greater than f) the amplitude of the signal is not affected, but the leading and trailing edges are distorted.

3. At frequency f_2 (which is greater than f_1) the signal is distorted and the amplitude is reduced.

4. At frequency f_3 (which is greater than f_2) the output is practically a steady state output at 5 ma.

NOTE - It should be clear now that distortion first affects the edges of a signal. Further increases in frequency reduce the signal amplitude; the hills are removed and the valleys are filled in. Also notice that the same amount of current reaches the collector, but the "change" of signal is reduced to almost zero.

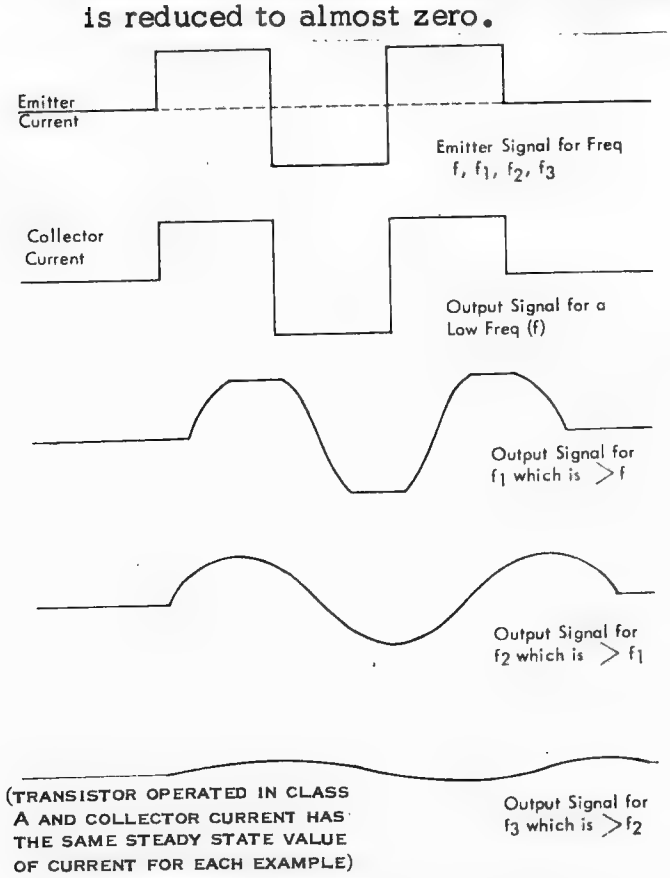


FIGURE 3.11 Frequency Response

1 Frequency Cut-off

In order to establish parameters dealing with frequency response, a response curve must first be drawn (Figure 3.12). Such a curve shows how the output signal is affected when the frequency is increased. Frequency is plotted on the horizontal axis and gain (the amount of output signal) is plotted on the vertical axis. The curve shows a uniform response until at some high frequency the gain falls toward zero.

The transistor frequency response is considered usable until it falls to a one-half power value. This value is .707 of its low frequency response and is referred to as the alpha cutoff frequency.

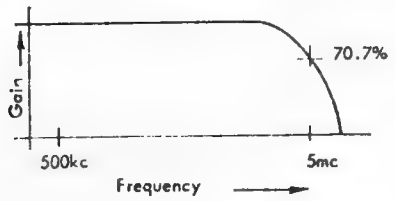


FIGURE **3.12** Frequency Cut-Off

It has been shown that frequency response is dependent on carrier transit through the base region. This is compared in Figure 3.13A & B showing that frequency response increases as the base width decreases.

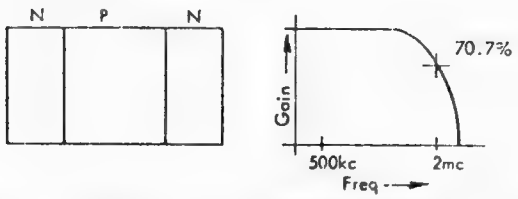


FIGURE **3.13A** Wide Base Region Results in Lower Frequency Response

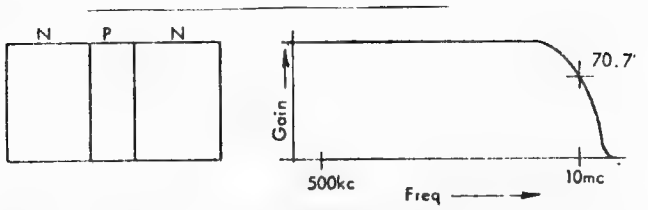


FIGURE 3.13B Narrow Base Region Results in High Frequency Response

Figure 3.14 shows the effect of forward bias when a PNP transistor is used. See how the forward biased emitter base junction has driven majority carriers to the barrier and reduced the depletion region to zero.

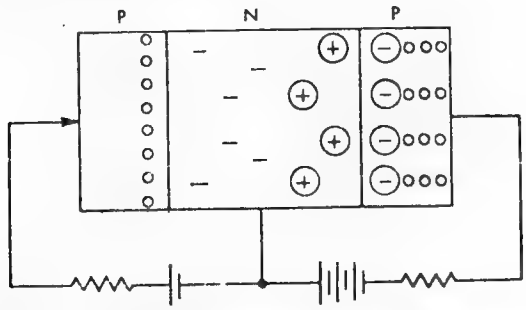


FIGURE 3.14 PNP Forward Biased Transistor

Electrons from the base enter the emitter (conduction band current), and holes from the emitter enter the base (valence band current). The hole enters the base when an electron from a neighboring germanium atom swings from orbit about the germanium atom to an orbit in the hole location. The emitter provides the major current source because it is doped more than the base.

In Figure 3.15 the emitter action is shown. Electrons are shown crossing the junction to fill holes in the emitter. The effect of such a transfer is that holes not appear in the base, so that it can be correctly stated that the emitter emitted holes into the base.

Frequency Cut-off (continued)

Holes entering the base become minority carriers and travel through the base region by diffusion. The holes move through the base and into the collector where the holes again become majority carriers and are strongly influenced by the negative source placed on the collector. Holes in the collector travel to the surface where they recombine with electrons delivered by the source. At the emitter terminal, electrons are released by the P-type impurity atoms. These electrons flow to the positive potential of the forward-bias source, and through it and the collector source and then to collector. Thus, electrons flow into the collector and out of the emitter. Atoms in the emitter then generate new holes which travel to the base region, and the current cycle continues.

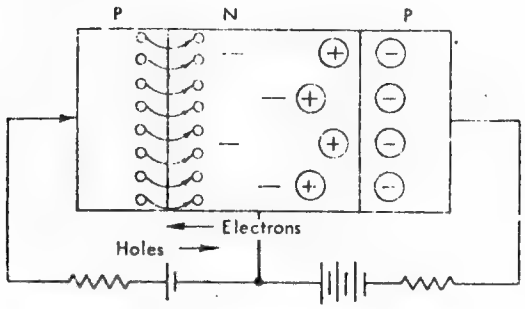


FIGURE 3.15 PNP Emitter Action

Basic Circuit Configurations

Transistor circuits have three basic circuit configurations that are similar to the three basic tube circuit configurations.

These are:

1. Grounded grid amplifier ═══ grounded or commoned base.

2. Grounded cathode amplifier (inverter) ═══ grounded or commoned emitter.

3. Grounded plate amplifier (cathode follower ═══ grounded or commoned collector.

Each of these circuits has certain characteristics which will be covered in detail in the study of each circuit. Each circuit has certain advantages over another. It is the utilization of these advantages which results in intelligent circuit design.

Grounded Base

The familiar grounded-grid amplifier is shown in Figure 3.16. In such an amplifier the signal voltage is applied to the cathode and the grid is held fixed or grounded. This circuit produces an output signal which is an amplified in-phase reproduction of the input signal. The transistorized version of this circuit is the grounded base shown in Figure 3.16. The circuit is so named because the input bias and the output bias are commoned to the base load.

Analysis of Figure 3-16 shows the following:

1. The B-to-E is forward biased.

2. I_e (emitter current) flows into the base where it divides into I_{be} (base-to-emitter current) and I_{ce} (collector-to-emitter current).

3. The input resistance (R_i) is small and the output resistance (R_l) is large.

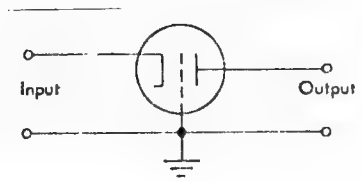


FIGURE 3.16 Grounded Grid Circuit

4. This circuit produces a current amplification (ration of output current to input current) of less than one (.98 shown), because some emitter current is lost to the base circuit (I_{ce} ═══ I_e ——— I_{be}).

5. A small input signal (current through R_i) produces a large output signal (current through R_l).

6. Because output current and input current are approximately equal, output voltage to input voltage is approximately equal to output resistance to input resistance. This ratio could be 100 to 1 or higher. Thus, this circuit is an excellent voltage amplifier.

Grounded Base (continued)

Current flowing in the collector circuit is called I_C (Figure 3.17). It consists of I_{ce} and I_{CO} (B-to-C reverse current). I_{CO} is a small current and is a function of junction temperature, not the potential applied. Normal signal levels (up or down) have little effect on I_{CO}, which is therefore a fixed amount (a constant). Thus, the output signal (change of signal level) is due to the change in I_{ce} and is not affected by I_{CO} which shows little to no change.

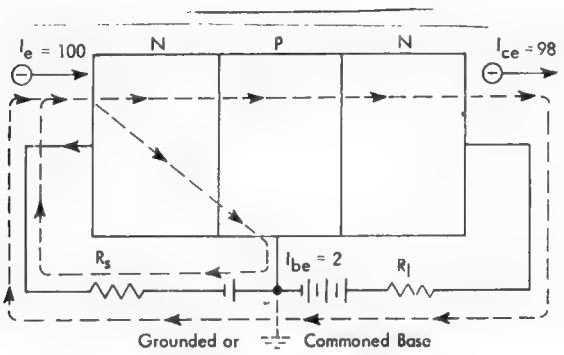


FIGURE 3.17 Grounded Base Transistor Action

SIGNED ASSYNCHRONOUS BINARY ADDER

CHAPTER 4

THE C T R L FAMILY OF SABA

CHAPTER 4.

THE CTRL FAMILY OF SABA

General

Combinational logic circuits can provide all of the logic functions necessary for computer circuits. Since transistors are used as the prime circuit element, as compared to diode circuits, these circuits are considered to be active, rather than passive as in the case with diode circuits.

The standard transistor configuration used, is the common emitter circuit. Since this is the case, the transistor used in the common emitter configuration, provides a direct invert function. By providing input circuits or gates, to the base of the transistor, both AND and OR functions can be performed.

Since both NPN and PNP transistors are available, complimentary circuits can be used to assist in the reduction of the number of logic functions or circuits that are required. Only PNP circuits are required in the SABA unit.

Also, since the transistor logic circuit is active, two or more of these circuits can be inter-connected so that they will perform a memory function, a circuit commonly known as a voltage mode trigger or latch. Combinational logic circuits inter-connected to perform a memory function are generally classified in a latch category.

Another definite advantage of transistor logic, is that two or more circuits may be connected together at their output terminals. Connecting outputs together gives an added advantage, in that it performs additional logic. All of these basic combinational logic circuits have been designed so that they may be inter-connected in many different configurations. They also have very definite loading stipulations to guarantee a high degree of reliability. Therefore, since these circuits must fall into a modular arrangement, they are found with two or three inputs. Many cases arise in computer logic where it is necessary to have a logic function with considerably more than two or three inputs. This requirement can be fulfilled by connecting the outputs in a manner similar to that described above.

Another advantage of the transistor logic circuits, is the fact that they only require two voltages, +12 volts and -12 volts.

CTRL Logic Levels

The type of logic used in the SABA unit is of CTRL type. CTRL is an abbreviation for Complementary Transistor Resistor Logic. In order to simplify the discussion of logic circuits used in computers, a method of shorthand notation for line levels has been developed.

CTRL logic levels can be divided into two parts. The first part are those circuits whose voltages, either input or output, shift between a positive voltage and a negative voltage. An 'R' is used to identify a positive voltage level. If the voltage level is a plus voltage level, (+6V to +12V) a plus symbol is used in front of the 'R', to designate a "+R" level. The "+R" level is defined as an inactive line level. It could be said that this represents a logic zero or an unconditioned state.

If the positive voltage level drops to ground, or just slightly above ground, this new level is still an 'R' level but is defined with a minus sign in front of the 'R', thus a "-R" level. The "-R" level defines a line that is conditioned or that the line is at a logic "1" or a conditioned level.

Voltages that operate between ground and a negative voltage are "S" levels. A negative voltage (from -6V to -12V) is defined as a -S level. The -S level present on a line, states that the line is not conditioned or is at a logic zero state. When the minus voltage level (-S) rises to a ground level, or just slightly below ground, the new level is defined as a +S level. A +S level conditions the line or represents a logic "1".

In CTRL Logic, when using combinational circuits, only 2 supply voltages are required. +12V and -12V provide the necessary potentials for operation of the various transistor circuits. (Figure 4.1 graphically explains the logic interpretation of the various voltage levels.) In the preceding discussion, both +6V and -6V were mentioned. When the logic of a computer uses AC operated triggers, then it is necessary to provide supply voltages of both +6V and -6V in addition to the +12V and -12V necessary for the operation of the combinational logic circuits.

CTRL Logic Levels (continued)

Summarizing, an "R" level defines a positive voltage level, and an "S" level defines a negative voltage level. Also, a + "R" level and a "-S" level are logically equal to each other or state that any line that is at this level is not conditioned.

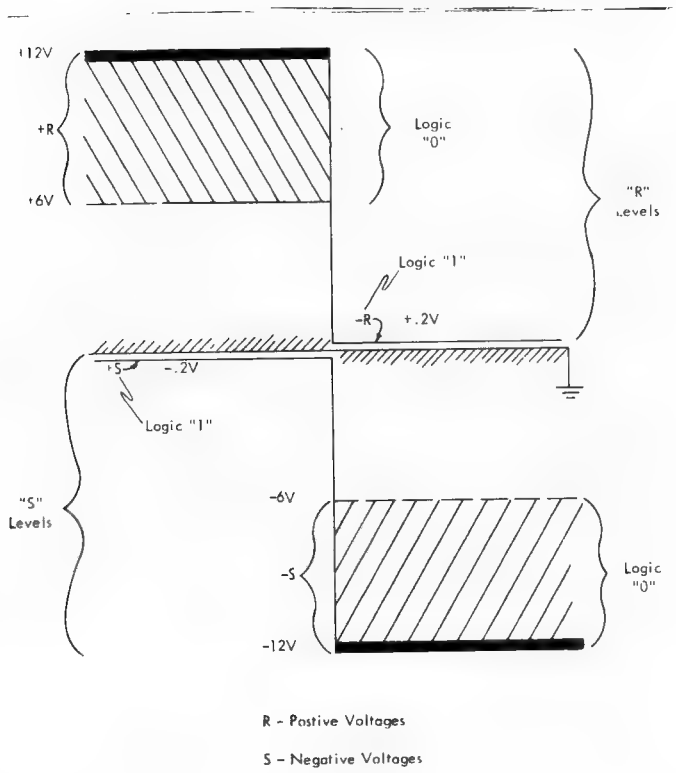


FIGURE 4.1 CTRL Levels

A "-R" level and a "+S" level are logically equal to each other and if present on a line or at the output of a circuit, state that the circuit or line is conditioned. In SMS CTRL Transistor Logic, the transistors are operated in one of two conditions. The first condition is that the transistor is in saturation and

CTRL Logic Levels (continued)

the second condition is that the transistor is cut off. Since these standard circuits may be inter-connected to perform various logic functions, the unconditioned output levels will vary between -12V and -6V or +12V and +6V, depending upon the external circuit loading. It can be said generally that if the output of a circuit when it is in the unconditioned state is not above +6V or not below -6V, will provide unreliable operation or even failure. The outputs of these transistor circuits will switch through this forbidden region, but should never be found in a steady state between +6V and ground or -6V and ground. When the transistor circuit provides a "-R" or +S level output, the transistor is providing the load current for the external circuit. In the SABA unit only the "S" level circuits are used.

The components used in CTRL logic, mainly the transistors, are low cost devices and consequently do not have an extremely high cut off frequency. The transistors used must be operated with large voltage swings and consequently when the transistor is driven into saturation, the circuit components will provide more base current than is actually required to keep the transistor into saturation. Over-driving the transistor results to some extent in a little bit longer turn-off time. Also, when the transistor is required to be in a non-conducting state, the bias is so arranged that the transistor is well beyond cut off. This also extends to some extent the turn-on time of the transistor. These facts can be summarized in the following way:

> By providing large voltage swings with CTRL transistor circuits, and staying below a 150 killocycles in frequency; these circuits are extremely reliable to both high usage and temperature.

NOR (N) Circuits

There are a variety of negative NOR circuits used in the SABA unit. These circuits are all similar in operation, but differ only in the number of inputs that are provided. Also, there are some circuits that provide logic directly into a second circuit, and these circuits are mounted on twin cards.

Nor (N), 2-Way, 4 Ckts

1. General

This NOR circuit provides two DC input gates, which provide for the combining of logic. The circuit transistor inverts this combined logic and provides the output. The inputs to this circuit must be provided with S levels. This circuit produces S level outputs and also provides for re-shaping and re-powering of the levels.

The card code for this circuit is MX and the SMS card contains four of these circuits. One circuit on the card does not have a collector load resistor and the reason will be explained later. There is, however, a resistor provided on the card that can be used as a collector load for any NOR circuit in the machine.

2. Circuit Description - Figure 4.2

This circuit can be sub-divided into two major parts. The first part consists of the two input resistors, input pins B and D, and the 43K base-bias resistor. This portion of the circuit provides for the "ANDING" of the two input signals. The second part of this circuit, the transistor which is used in a common emitter configuration, can be classified as an inverter circuit. The output is taken directly from the collector, pin G.

2. Circuit Description (continued)

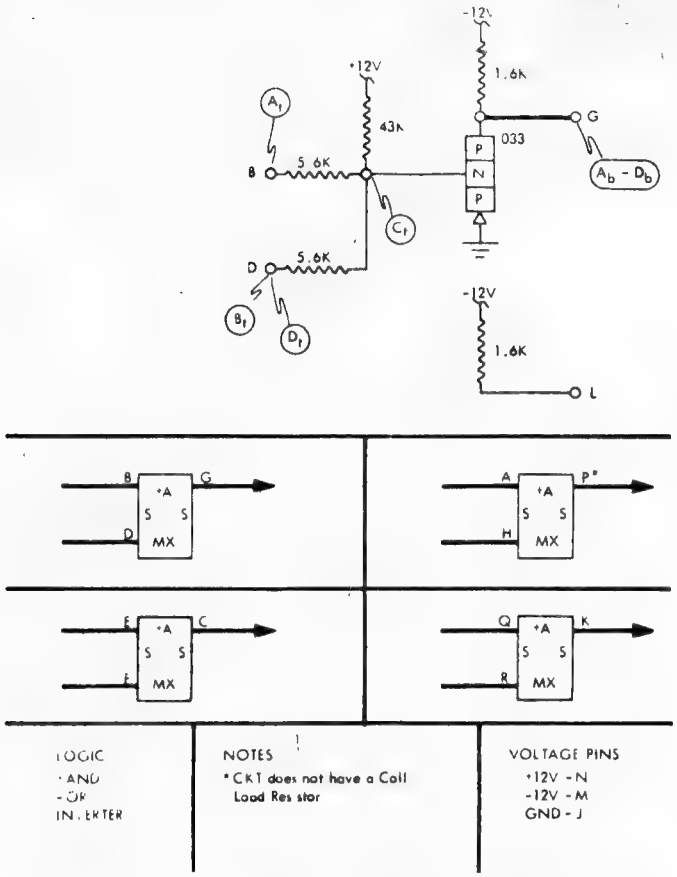


FIGURE 4.2 NOR (N), 2-Way, Circuit & Logic

The output level at pin G, depends directly upon the levels at the inputs. Since this circuit has two input gates, pins B and D, there are four situations that can occur. The first situation can be shown in Figures 4.3A and B. Both inputs to the DC gates are at ground levels. This provides a -9V level output at pin G. With both pins B and D at ground level, the voltage division between the two 5.6K input resistors and the 43K base-bias resistor provide a positive voltage at point C. Referring to Figure 4.3C, the voltage on the base of the 033 transistor is at approximately +.5 volts. With the emitter of the transistor connected to ground, this provides a reverse biased potential across the

2. Circuit Description (continued)

base emitter junction. The transistor is cut off and the output voltage will be negative, up to -12Volts. The level of the out-put voltage with the transistor cut off, will depend on a external load connected to this circuit.

If either pin B or D is driven below ground (-S levels), the condition of the circuit changes. In Figure 4.3B, the input to pin D drops to -6V. Now the potential at this division of voltage is again associated with the 2 input resistors and the base-bias resistor. However, as the voltage on the base of the transistor goes below ground, the transistor becomes forward biased. In Figure 4.3C, the base of the transistor has been clamped to about -.4V.

This is due to the diode action between the base and the emitter. This negative potential on the base is sufficient to hold the transistor fully in saturation and current flows through the transistor and its collector load. With the transistor in saturation, the drop across the device becomes very small and can be neglected for practical purposes. Therefore, with pin D going to a negative voltage, the output at pin G rises to ground as the transistor goes to saturation. The transistor is now supplying the external load current for the circuits that are connected to its output.

The same situation also exists if pin D remains at ground, but pin B goes to a negative voltage. This can also be seen in the scope waveforms of Figures 4.3A and B. The last of the four situations of input voltages that can occur, is to have both inputs driven to a negative voltage level. However, when this occurs, the base is driven further negative, increasing the forward bias. The transistor clamps the base close to ground, and the output assumes a ground level.

To summarize, with either of the inputs at a negative

2. Circuit Description (continued)

voltage, the output will be at ground level. When both inputs are at a ground level, the output will be at a negative voltage level. When both inputs are negative, more base current is allowed to flow, and therefore, at this time requires the greatest amount of input current.

In Figure 4.3D, the oscilloscope picture has been expanded to show the delay time involved in this circuit. The top trace is the voltage pulse at the D input pin and the bottom trace is the output at pin G. Notice that the turn-off time of the input pulse is just slightly less than .3 of a microsecond and the turn-on time of this circuit is just slightly less than .4 of a microsecond. The actual turn-on delay time will be computed as the difference between the 90% point on the curve and the 10% point. Both the turn-on and turn-off delay time is a direct function between the input and output voltage levels as well as the loading on this circuit.

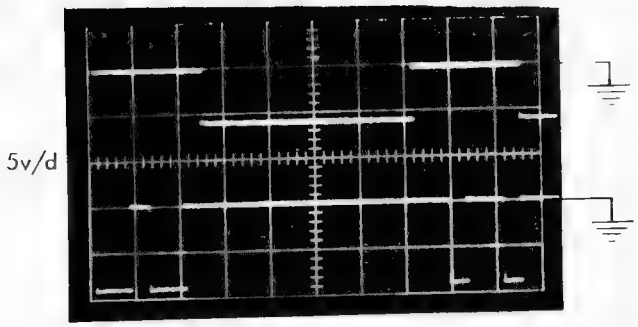


FIGURE 4.3A Input Pin B vs. Output Pin G

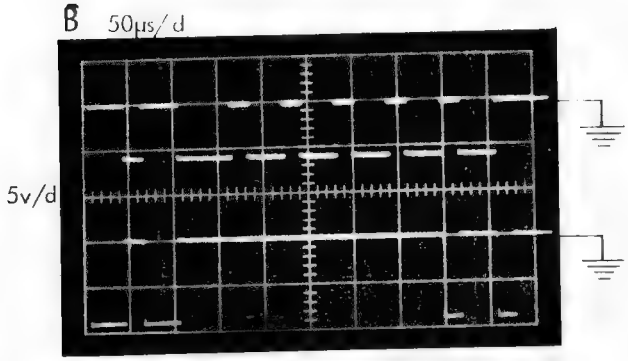


FIGURE 4.3B Input Pin D vs. Output Pin G

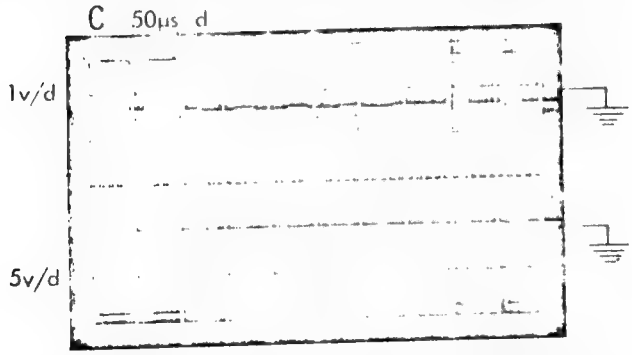


FIGURE 4.3C Transistor Base vs. Collector

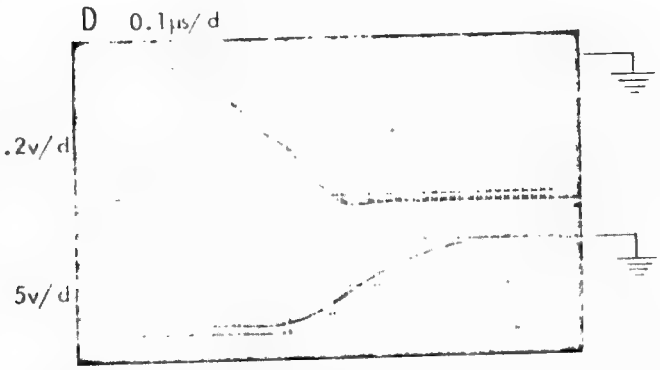


FIGURE 4.3D Transistor Circuit Delay Time

Nor (N) 2-Way, 4 Ckts

3. Logic

The logic performed by the N NOR circuit is sufficient to implement all functions required in a computer. However, as previously explained, a considerable reduction in components can be made by using complementary circuits. The discussion that follows in NOR (N) logic will apply to all NOR circuits used in the SABA unit.

Figure 4.4 shows a photograph of the component side and the wiring side of this particular circuit. The card code is MX and contains four of these circuits. The circuit with output P does not have a collector load resistor, however, a 1.6K resistor is provided with an output to L, and it can be used with this circuit or another similar circuit elsewhere. This circuit performs +AND, -OR, or if only one input is used, invert logic. To best understand the logic formed by this circuit, refer to Figure 4.5, a truth table for this circuit. State 1 will assume that both input pins, B and D, are at -S levels. This will produce a +S level on the output at pin G. The next state, 2, pin B has gone to a +S level while pin D remains at a minus S level. The output remains unchanged, that is, at a +S level. In state 3, the levels on the input pins have been reversed, and the output remains at a +S level. In state 4, both inputs are now at a +S level, and the output has changed to a -S level. These are all of the possible combinations of input line levels for this circuit.

Notice that for states 1, 2 and 3 the output remained at a +S level. Stating this in another way, if any one of the inputs is at a -S level, then the output will be at a +S level. Therefore, three of the 4 states provide an OR FUNCTION. Since the rule states that any one of the inputs must be at a -S level, then this circuit performs -OR logic. The only state of the truth table that causes the output to go its one and only different level, that is a -S level, is the 4th state. When this circuit utilizes the 4th state, then the circuit performs a +AND function, since both of the inputs are at +S levels. It should be noted that the circuit really has two names, -OR or +AND. The logic designer will

Nor (N) 2-Way, 4 Ckts (continued)

3. Logic (continued)

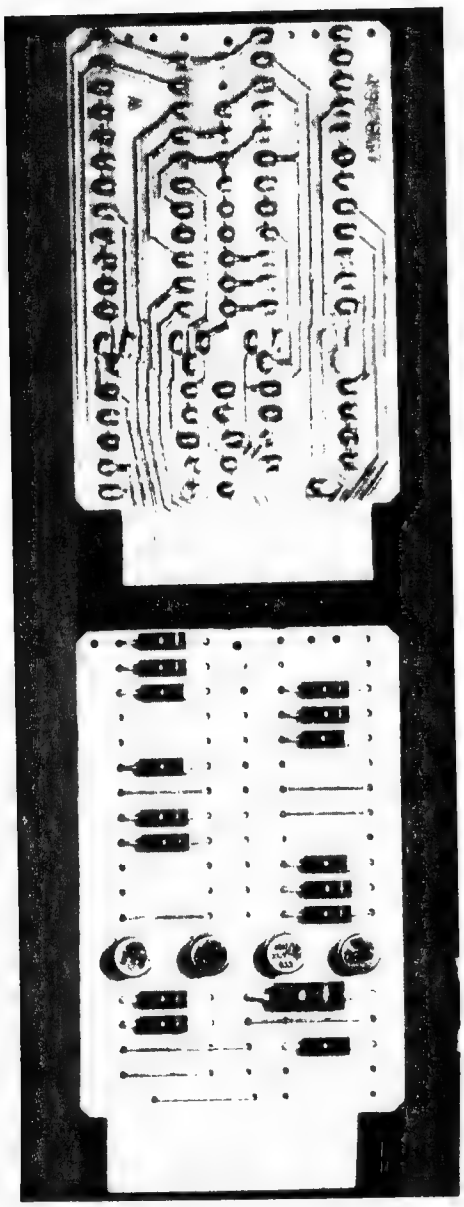


FIGURE 4.4 MX SMS Card

Nor (N) 2-Way, 4 Ckts (continued)

3. Logic (continued)

State	Input B	Pins D	Output Pin G	Logic
1	-S	-S	+S	-OR
2	+S	-S	+S	
3	-S	+S	+S	
4	+S	+S	-S	+AND

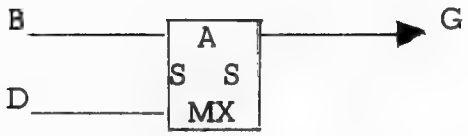


FIGURE: 4-5 - NOR Block and Truth Table

will decide which name the circuit should receive when the logic is designed. The name that is given to this circuit will depend upon what line level is desired on the output.

The 3rd function performed by this circuit is that of an inverter. If the circuit had only one input or had one of the two inputs grounded, then the circuit would perform a direct invert function.

There may be times when the logic designer needs one of the circuits that has more than the number of inputs available. To expand the number of inputs for this type of logic circuit, all that is necessary is to connect the collectors of the circuits together. However, there can be only one collector load resistor which is then common to each of the circuits. This is the reason that on this particular card, there is one circuit that does not have a collector load resistor as an integral part of the circuit. In figure 4.6, two of the circuits have been connected so that 4 inputs are now available.

3. Logic (continued)

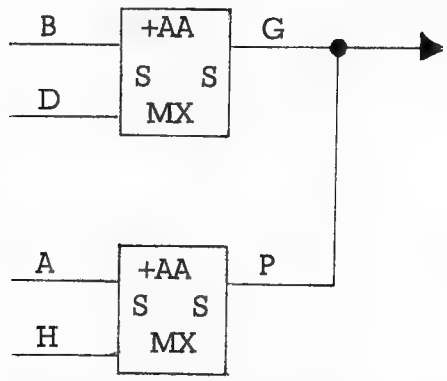


FIGURE: 4-6 - Dot Function

Connecting the collector outputs together is sometimes called "ORING" outputs, or dot functioning the outputs together. A number of these circuits can be dotted together providing a greater number of inputs.

The logic name of these circuits again has been decided by the circuit designer, and it depends upon what the output level must be. Referring to Figure 4.7, a truth table has been written for the logic of the two circuits dotted together in Figure 4.6. With 4 inputs, there are 16 possible states. Each of the input states are shown as well as the state of the individual circuit and the state of the common output line. Notice that states 1 through 15 all provide +S levels at the common output. Of these 15 various states, those that are checked, 6, 7, 12, 13, 14, and 15, one of the circuit outputs are at a +S level. When either circuit output is at a +S level, this will override the other circuit output at a -S level. These first 15 states define the circuit in terms of a -OR function. The only set of input states that will provide a common output line change from +S to -S is the 16th state. This is the +AND function condition.

3. Logic (continued)

State	Input Pins				Output Pins		
	B	D	A	H	G	P	Common
1	-S	-S	-S	-S	+S	+S	+S
2	+S	-S	-S	-S	+S	+S	+S
3	-S	+S	-S	-S	+S	+S	+S
4	-S	-S	+S	-S	+S	+S	+S
5	-S	-S	-S	+S	+S	+S	+S
6	+S	+S	-S	-S	-S	+S	+S
7	-S	-S	+S	+S	+S	-S	+S
8	+S	-S	-S	+S	+S	+S	+S
9	-S	+S	+S	-S	+S	+S	+S
10	+S	-S	+S	-S	+S	+S	+S
11	-S	+S	-S	+S	+S	+S	+S
12	+S	+S	+S	-S	-S	+S	+S
13	-S	+S	+S	+S	+S	-S	+S
14	+S	-S	+S	+S	+S	-S	+S
15	+S	+S	-S	+S	-S	+S	+S
16	+S	+S	+S	+S	-S	-S	-S

FIGURE: 4-7 - Truth Table for a Dot Function

In Figure 4.8, the two circuits that have been under study, being dotted together, are shown with various logic names. As is the case with the first 2 logic circuits, double letter notation has been used to describe the logic function that they perform. The first letter in each block, +AND or -OR, designate the desired levels of the inputs to that particular block. It also establishes the logic that the block forms. The second letter of a double letter blocks, indicates what logic is performed between the two blocks that are dotted together. From the blocks drawn in the first 2 sketches it can be seen, there are more than one possible combinations of logic interpretation of the same circuits. The next two dotted blocks, one with a +A and the other with a -OR, show the second block with an E. This stands for "Extender", and means that the circuit performs a +AND function, however, additional inputs were required, so therefore the block extends the number of inputs. This is true in the case of the -OR, as it also has been extended for additional inputs. The last two group of blocks show how an inverter function can be "ANDED" or "ORED" by dotting the outputs of the circuits concerned together. In the case of using as the first letter an '1' it is not necessary to indicate the sign.

Nor (N) 2-Way, 4 Ckts (continued)

3. Logic (continued)

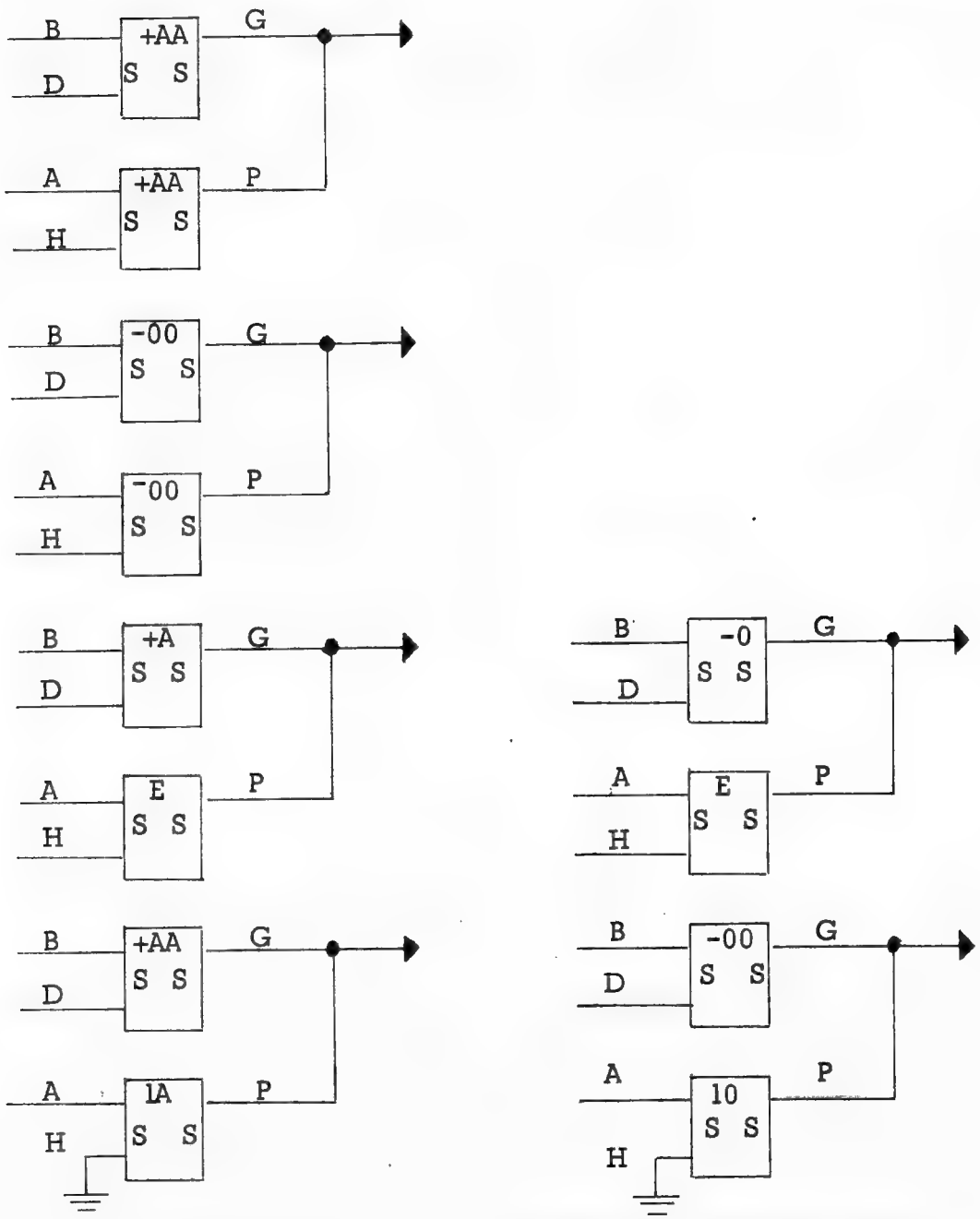


FIGURE: 4-8 - Dot Function Logic Configurations

Another significant use of these circuits can be made by connecting the outputs of 2 of these circuits back to one of the opposite inputs of the other circuit, Figure 4.9. When the outputs are connected back as shown in Figure 4.9, the circuit is termed a latch. This is a form of a trigger which is DC level operated or operates on leading edge response logic. It is possible to obtain a latch-up of this circuit because of the transistors

3. Logic (continued)

employed, these being active circuit elements. The latch is drawn in this configuration because the top block represents the ON circuit and the bottom block represents the OFF circuit. Correspondingly, the top output is the ON output of the latch and the bottom output is the OFF output of the latch. Input B of the top block is generally referred to as the set line and input F of the bottom block is the reset line.

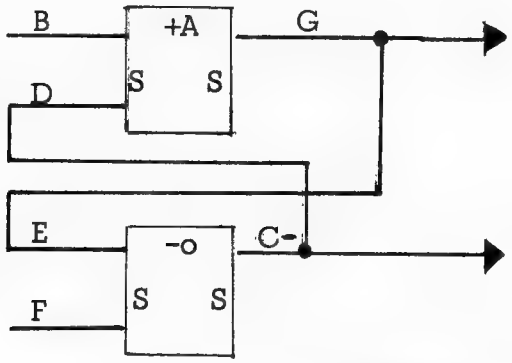


FIGURE: 4-9 NOR Latch

To best describe the function of this circuit device, refer to its truth table in Figure 4.10. The logic name of each of the blocks again has been applied to the discretion of the logic designer in the way in which the circuit performs. For illustrating this example, the top block has been chosen to be an +AND block and the bottom a -OR block. Starting with state 1, both inputs have been placed at a +S level. Since it is not known what the previous state of the latch was, or it is not known in which way the latch will become setup when power is applied, no assumptions can be made as to the levels of their outputs. Therefore the levels of pins G and C are indeterminate at this time. This is a problem that must always be taken into account when studying the various circuits of SABA. It also must be recognized that there must also be a beginning condition or beginning set-up conditions, so that the states of the latch can be established.

3. Logic (continued)

Since pin F has been assigned the job of reset, B being the set line, state 2 in the truth table takes pin F to a -S level. With pin F going to a -S level, the bottom block, or the-OR function is satisfied and the output C-L rises to a +S level. This +S level is latched back through pin D, to one of the inputs of the ON block. Now both pins, B and D, are at +S levels. This satisfies the +AND function of the ON block, and provides a -S level output. The -S level output at pin G is latched back to pin E, one of the inputs of the OFF block. Since the OFF block performs a minus OR function, both inputs are now at -S levels and the output remains unchanged. At this point, the status of the latch has been determined and it is said that the latch is OFF, since the ON output is at a -S level, and the OFF output is at a +S level.

State 3 of the truth table shows the complete latching situation of this circuit. When the reset line, pin F, is returned to a +S level, the -OR function of the OFF block remains satisfied by virtue of the -S level on pin E.

State	Input Pins		Output Pins	
	B	F	G	C-L
1	+S	+S	?	?
2	+S	-S	-S	+S
3	+S	+S	-S	+S
4	-S	+S	+S	-S
5	-S	+S	+S	-S
6	-S	-S	+S	+S

FIGURE 4-10 NOR Latch Truth Table

Therefore, in state 3, as pin F rises to a +S level, the output of both the ON and OFF blocks remains in a status by where the latch is held in an OFF condition. The latch now remains OFF until further action takes place and can be considered as a DC operated trigger.

Since the latch is OFF, any further action with pin F, the reset line, could not cause the latch to change state. Therefore, proceeding to state 4 of the truth table, input pin B, the set line, is brought to a -S level. When pin B drops to a -S level, and +AND function of the ON

3. Logic (continued)

block is no longer satisfied. The output of the ON block, pin G, rises to a +S level. The level on pin G is latched back to pin E of the OFF output block and with both pin E and pin F at +S levels, the -OR function of the OFF block is no longer satisfied. the OFF output, pin C, is latched back to pin D of the ON block. The level of the OFF output has now dropped to a -S level. At this point, the latch has been turned ON, as the ON output is now a +S level and the OFF output is now at a-S level. In state 5 of the truth table, the set input line has been returned to its previous level. This again does not affect the status of the latch, since the off output is holding pin D at a -S level.

There is one additional state of input conditions that can be applied to the latch that are illegal or redundant. Referring to the truth table, in state 6, if both inputs B and F are brought to -S levels, they will in turn hold the respective block outputs at +S levels, regardless of the latch backs. If both the on output and the off output are at +S levels, it cannot be stated whether the latch is on or off. Therefore, this situation must never happen.

To summarize, the logic of a N-type NOR circuit can be a +AND function or a -OR function. If only one input is used, then the circuit is classified as an inverter. Remember, that both inputs and outputs operate at S levels. Only circuits that have S level outputs can drive this circuit and this circuit can drive only those circuits whose inputs accept S levels. Figure 4.11 illustrates the shorthand notation of the logic formed by this circuit.

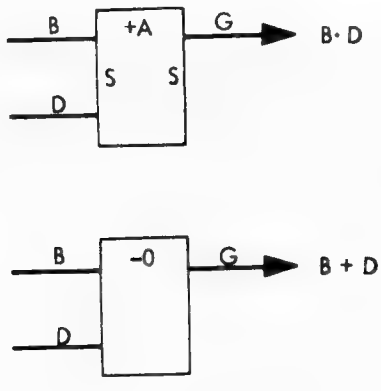


FIGURE: 4.11 NOR Circuit Logic

Nor (N), 2-Way, 4 Circuits (No Collector Load Resistors)

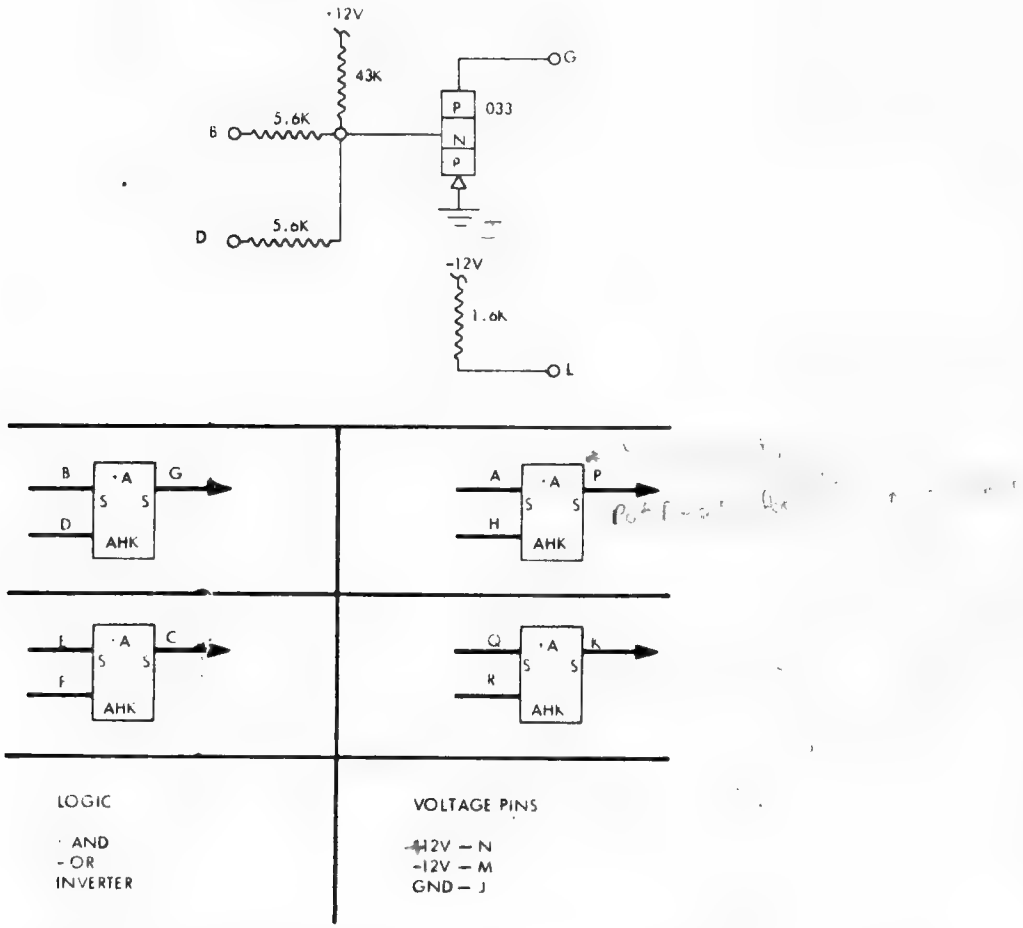


FIGURE 4.12 NOR (N), 2-Way, (No Collector Load Resistors) Circuit & Logic

This circuit, shown in Figure 4.12, is almost identical to the preceding circuit. The only difference between this circuit and the preceding circuit is the fact that none of the individual circuits on this card have the collector load resistor provided. All of the circuits on this card are designed to be used with circuits that have S level outputs and a load resistor. They provide additional inputs for or become an extension of the block with which they are dotted. Figure 4.13 is a picture of the component side and wiring side of the card.

Nor (N), 3-Way, 3 Circuits

This Nor circuit is provided with 3 inputs and is illustrated in Figure 4.14. There are three of these circuits on this card and one, with output pin C, does not have a collector load resistor. A separate collector load resistor is provided at pin L. This circuit also performs +AND, -OR, and Invert Logic in the same manner that the 2-way input Nor circuit functions.

The card code for this card is CD and a photograph of the component side and the wiring side is shown in Figure 4.15.

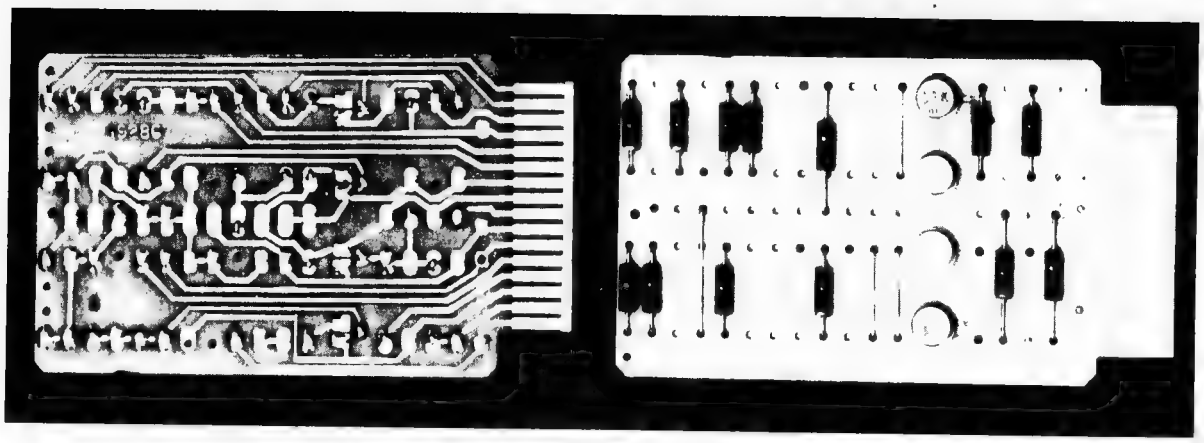


FIGURE 4.13 AHK SMS Card

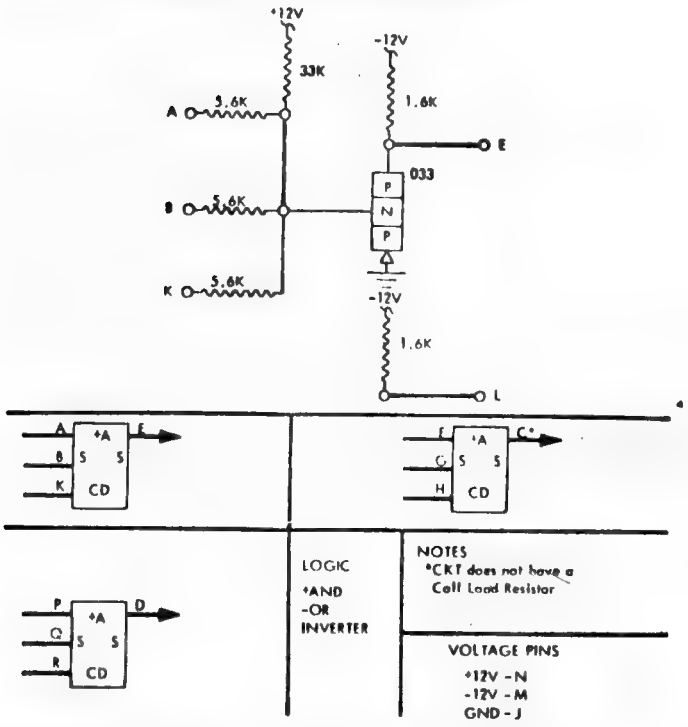


FIGURE 4.14 NOR (N), 3-Way, Circuit & Logic

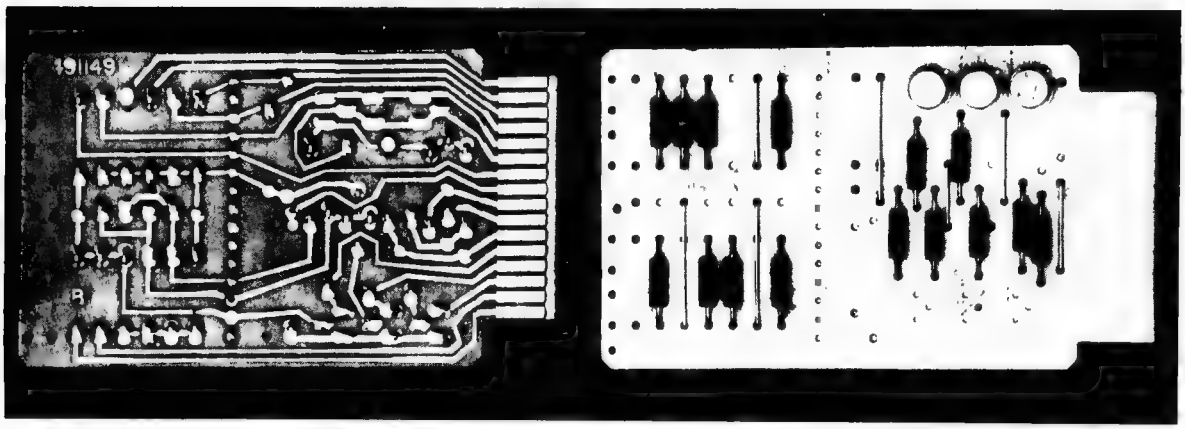


FIGURE 4.15 CD SMS Card

Nor (N), 3-Way, 3 Circuits (No Collector Load Resistors)

This Nor circuit is identical to the preceding circuit, however, none of the 3 circuits on this card have a collector load resistor, Figure 4.16. Each of the three circuits have 3 inputs, and the circuit is used primarily for extending the input capacity of a similar circuit. A separate collector load resistor is provided at pin L and the card code for this card is CAB. The logic performed by these circuits is +AND, -OR, and Invert. The photograph of this card is shown in Figure 4.17.

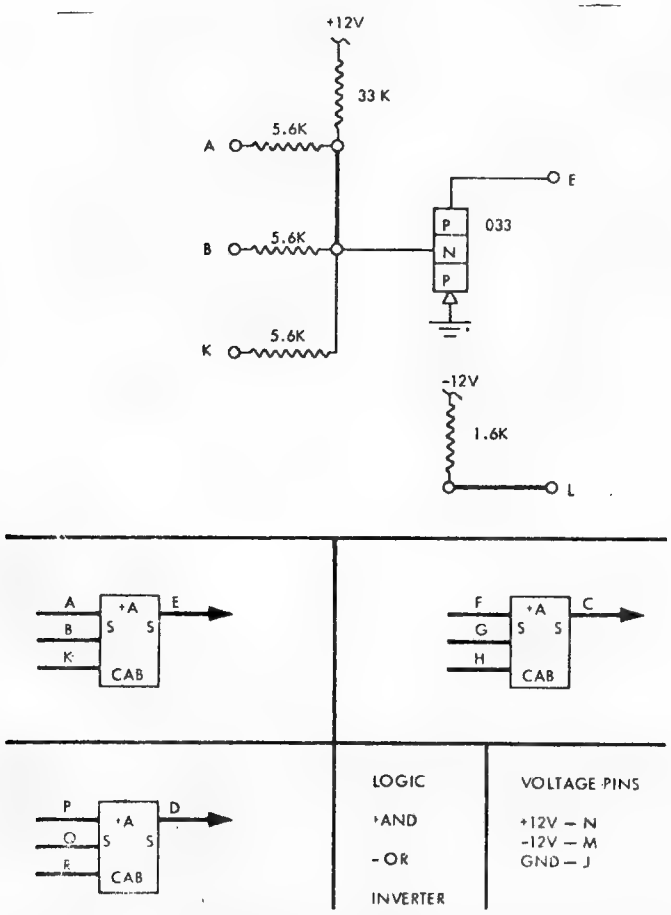


FIGURE 4.16 NOR (N), 3-Way, (No Collector Load Resistor) Circuit & Logic

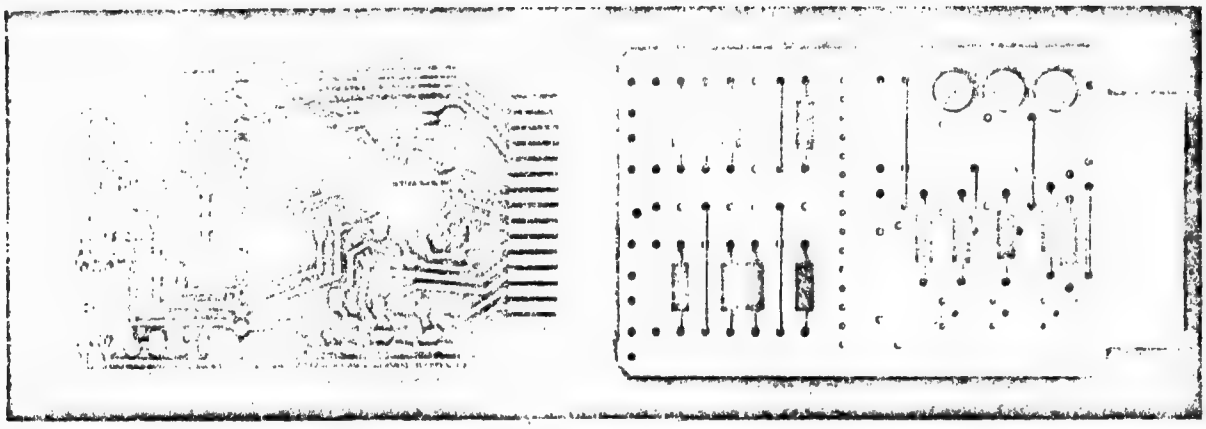
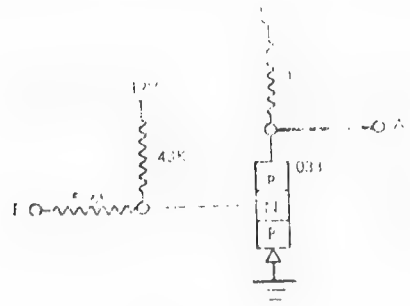


FIGURE 4.17 CAB SMS Card

Nor (N), 1-Way, 6 Circuits.

The circuit for this card is illustrated in Figure 4.18. This card provides 5, one-input circuits, and one two-way input, S to S circuit. The inverter circuit with output pin B does not have a collector load resistor. The logic performed by these circuits is a direct invert function, however, the two-way input circuit performs +AND, -OR, and Invert logic. The card code for this card is AKV and a picutre of the card is shown in Figure 4.19

Nor (N), 1-Way, 6 Circuits (continued)



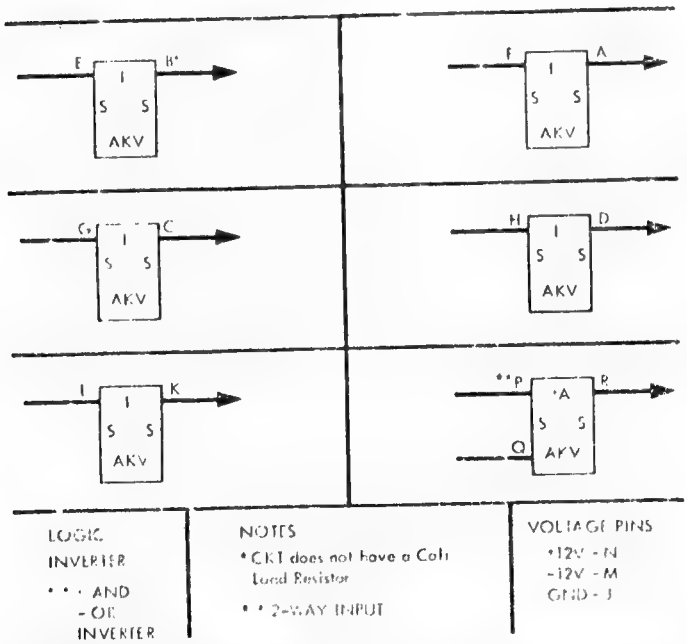


FIGURE 4.18 NOR (N), 1-Way, Circuit & Logic

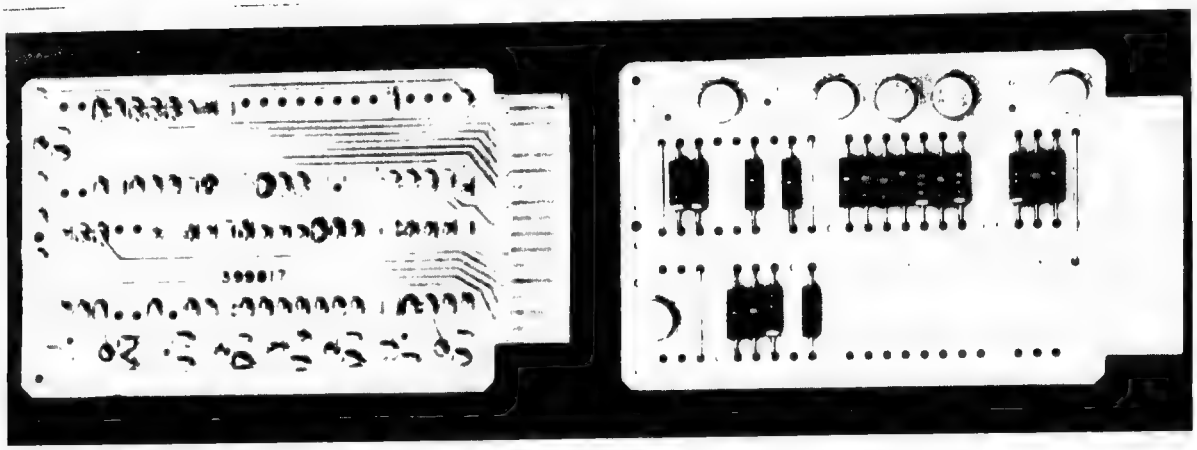


FIGURE 4.19 AKV SMS Card

Nor (N), 2-3 Way, 5 Circuits

1. Circuit and Card Description

This card contains 5, 2-3 Way, S to S level circuits. These circuits are contained on a twin card. The circuit diagram and the logic blocks with pin notations are shown in Figure 4.20. Even though the 2-Way circuit is connected directly on the card to one of the inputs of the 3-Way circuit, the logic block drawn in the systems prints will show 2 separate blocks. This type of an arrangement allows more logic circuits to be mounted on one card with a reduction in the number of SMS Card receptacles.

Notice that several of the circuits do not have a collector load resistor provided. Also, several of the circuits have the output of the 2-Way block brought out to an external pin. Two of the circuits do not have this output externally available, and this has been shown with a star (*). A separate collector load resistor is available at Pin A on this card, and a photograph of this twin card is shown in Figure 4.21

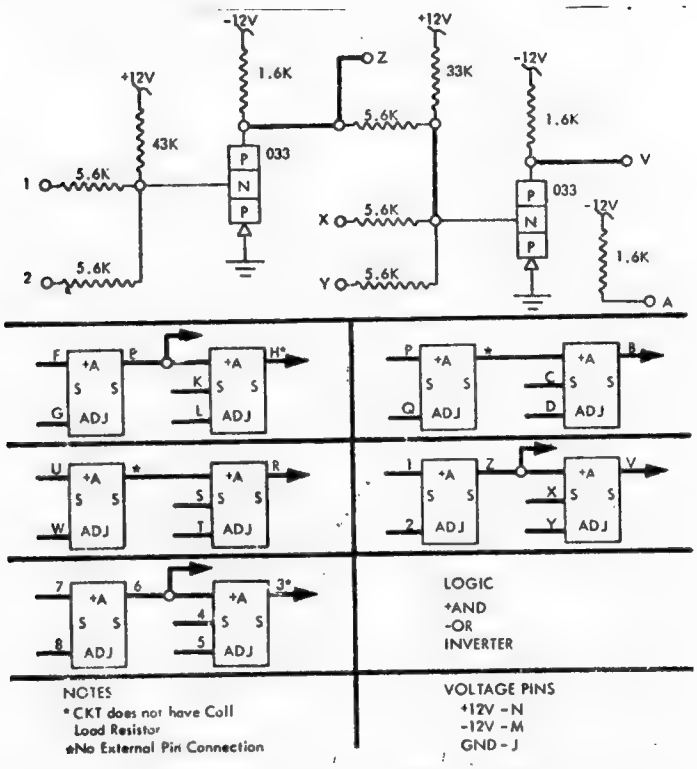


FIGURE 4.20 NOR (N), 2-3 Way, Circuit & Logic

Nor (N), 2-3 Way, 5 Circuits (continued)

1. Circuit and Card Description

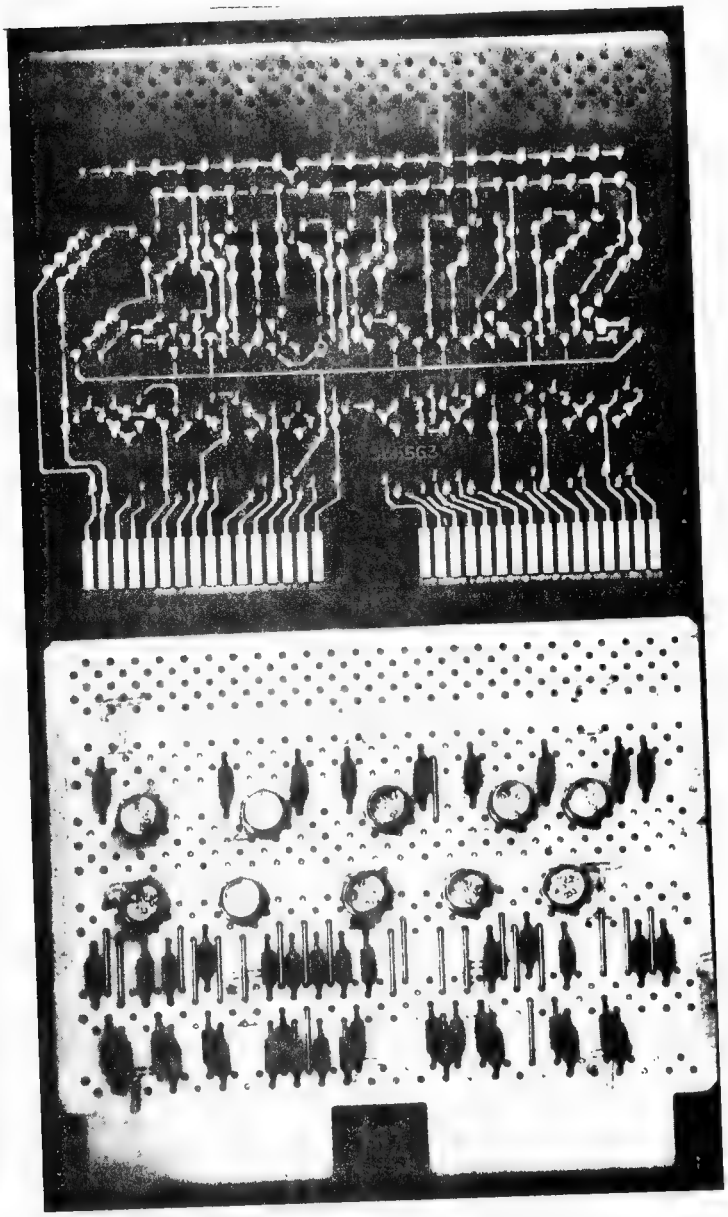


FIGURE 4.21 ADJ SMS Card

2. Logic

The over-all logic performed by this circuit can be best shown by using a truth table, Figure 4.22. The truth table has shown the conditions on inputs 1 and 2, generating the states available at output pin Z and also available to input Z of the 3-Way block. The truth table has been extended for all possible combinations of input levels on the 3 input circuit. Also, Figure 4.23 expresses the logic performed by this circuit in a shorthand method of notation. The over-all logic found at output pin B consists of the direct ANDING of inputs 1 and 2 "ORED" with both the complement of X and the complement of Y. It is possible to see that these circuits can be very useful in combinational logic and in many cases, are used as NOR Latches.

2-Way Block Inputs		3-Way Block Inputs Output			Output
1	2	Z	X	Y	V
+S	+S	-S	-S	-S	+S
-S	+S	+S	-S	-S	+S
+S	-S	+S	+S	-S	+S
-S	-S	+S	+S	+S	-S
		+S	-S	+S	+S
		-S	+S	+S	+S
		-S	-S	+S	+S
		-S	+S	-S	+S

LOGIC

$Z = \overline{1} + \overline{2}$

$V = \overline{Z} + \overline{X} + \overline{Y} = \overline{(\overline{1} + \overline{2})} + \overline{X} + \overline{Y}$

$= 1 \cdot 2 + \overline{X} + \overline{Y}$

FIGURE: 4.22 - NOR (N), 2-3 Way Truth Table

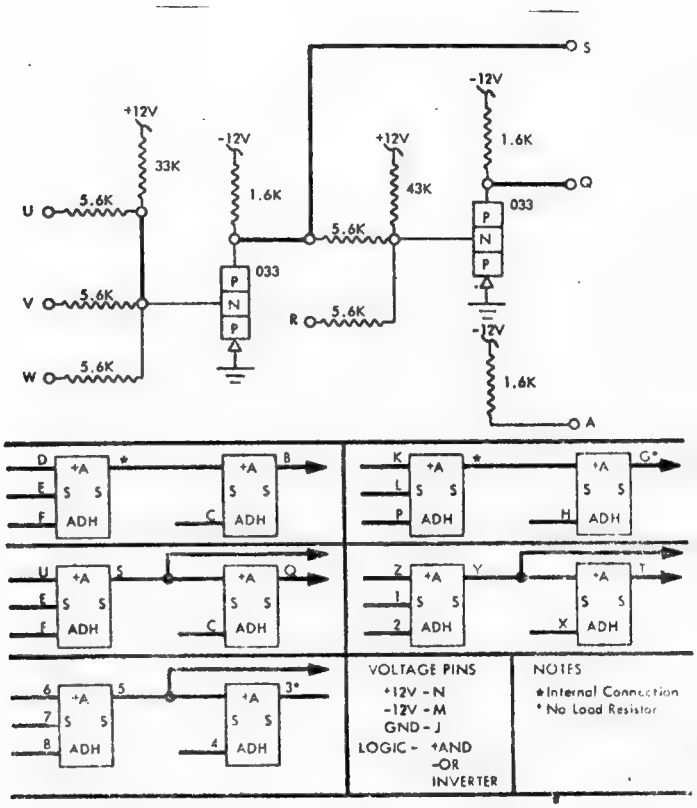


FIGURE: 4.23 - NOR (N), 3-2 Way Circuit & Logic

Nor (N), 3-2 Way, 5 Circuits

1. Card and Circuit Description

This twin card, with card code ADH, also provides 5 double circuits, Figure 4.24. The circuits on this card provide 3-Way, S to S level blocks driving 2-Way S to S level blocks. Several of the circuits have the internal connections between blocks brought out to an output pin. Two of these circuits do not have this inside connection available at an output pin. Also, two of the two-way output circuits do not have a collector load resistor. There is, however, a collector load resistor provided on outpin pin A. The picture of this card is shown in Figure 4.24.

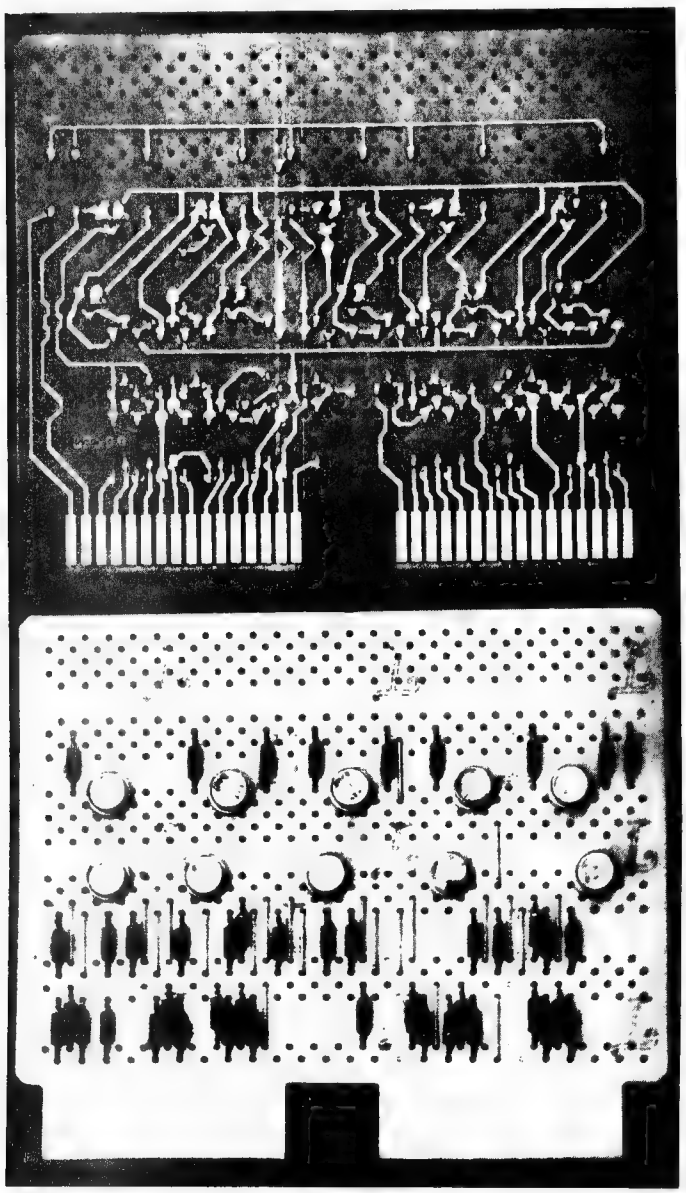


FIGURE 4.24 ADH SMS Card

Nor (N), 3-2 Way, 5 Circuits (continued)

2. Logic

A truth table has been used to show the various states that the inputs can assume for this circuit and indicates what the two outputs will be for these situations. The logic performed by this circuit provides for an "ANDING" of the 3 inputs of the first circuit, then "ORING" this output with the complement of the second input of the second circuit as shown in Figure 4.25.

Truth Table

3-Way Block Inputs			2-Way Block Inputs		
			Output		Output
U	V	W	S	R	Q
+S	+S	+S	-S	-S	+S
-S	+S	+S	+S	-S	+S
+S	-S	+S	+S	+S	-S
+S	+S	-S	+S		
-S	-S	+S	+S		
+S	-S	-S	+S		
-S	+S	-S	+S		
-S	-S	-S	+S		
Logic			-S	+S	+S

$S = \overline{U} + \overline{V} + \overline{W}$

$Q = \overline{S} + \overline{R} = \overline{(\overline{U} + \overline{V} + \overline{W})} + \overline{R}$

$= U \cdot V \cdot W + \overline{R}$

FIGURE 4.25 NOR (N), 3-2 Way, Truth Table

Inverter, Power (N), 6 Ckts

1. General

This circuit is used for distribution of a signal where a large number of circuits are to be driven. It requires S level inputs, and provides S level outputs.

2. Circuit Description

This circuit is similar to the NOR inverter circuit, that is, if a +S signal is applied at the input, pin G, the division of voltage between the 2K input resistor and the 33K base bias resistor will provide a positive

2. Circuit Description (continued)

potential on the base of the transistor, Figure 4.26. Referring to the bottom trace of Figure 4.26A, the base potential will be at a +.8 Volts. This will reverse bias the base-emitter junction of the transistor, and provide a -12 Volt to a -6 Volt output on pin D, Figure 4.26B, bottom trace. The output voltage on pin D will vary between -12 and -6 Volts, depending upon the external circuit load.

When the input voltage on pin G drops to a - S level, -6 to -12 Volts, the division of voltage between the 2K and the 33K resistors will attempt to drive the base of the transistor negative. This forward biases the base-emitter junction, and by diode action, the base of the transistor is clamped to about -.4 Volts, Figure 4.26A, bottom trace. When the base-emitter junction becomes forward biased, the transistor will conduct and provide a ground level on the output pin.

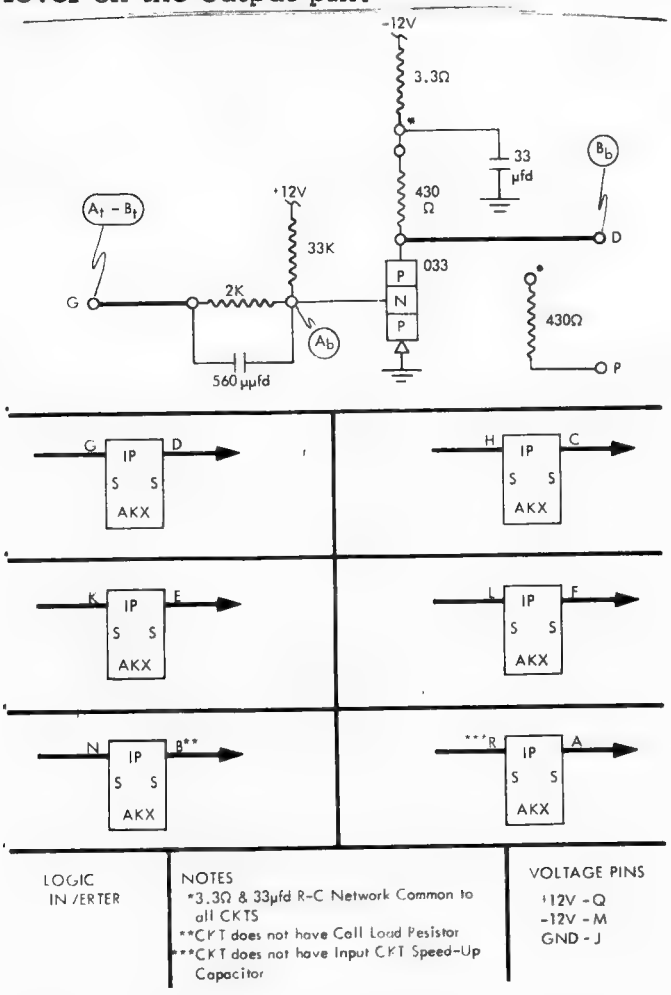


FIGURE 4.26 Inverter, Power (N), Circuit & Logic

2. Circuit Description (continued)

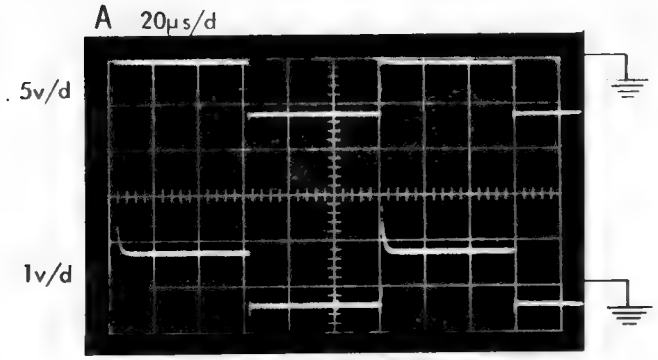


FIGURE 4-26A Input vs. Output

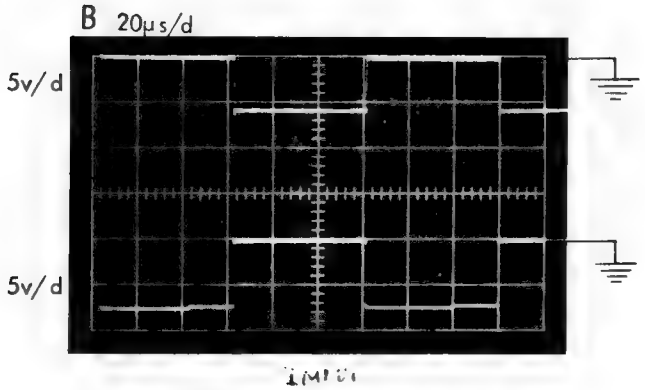


FIGURE 4.26B Base vs. Collector

Each of these circuits has the -12V collector supply decoupled with a 3.3Ω and a 33 μfd capacitor. This decoupling network is common to all circuits on this card. The circuit with output pin B does not have a collector load resistor.

The capacitor connected across the input resistor, is often called a speed -up capacitor. The greatest effect of the speed-up capacitor is felt when the input voltage on pin G rises to ground. This positive shift is peaked by the capacitor and assists in turning off the transistor, and provides a fast turn-off of the output circuit. The circuit with input pin R, does not have a speed-up capacitor

Inverter, Power (N), 6 Ckts (continued)

3. Logic

This circuit provides direct S to S level invert logic. The card code for this card is AKX and a photo of the card is shown in Figure 4.27.

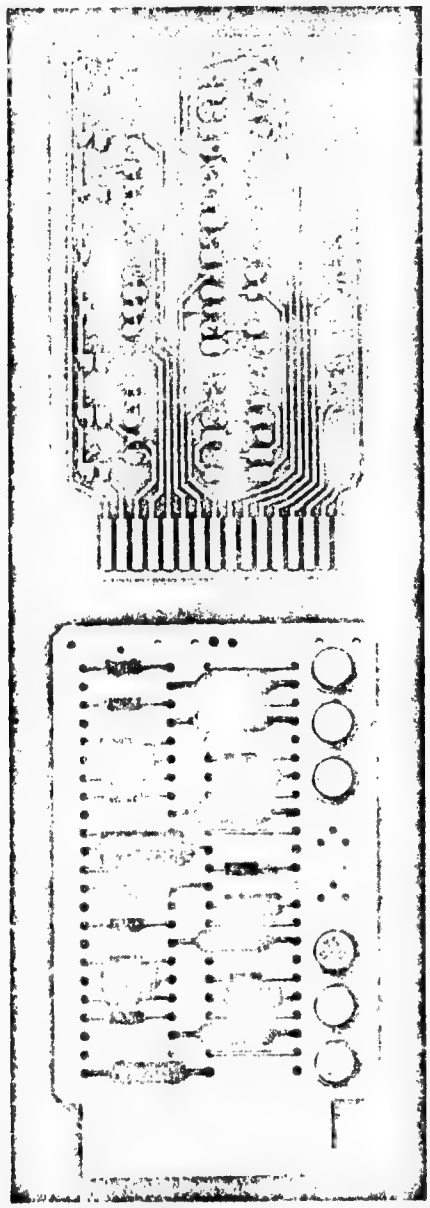
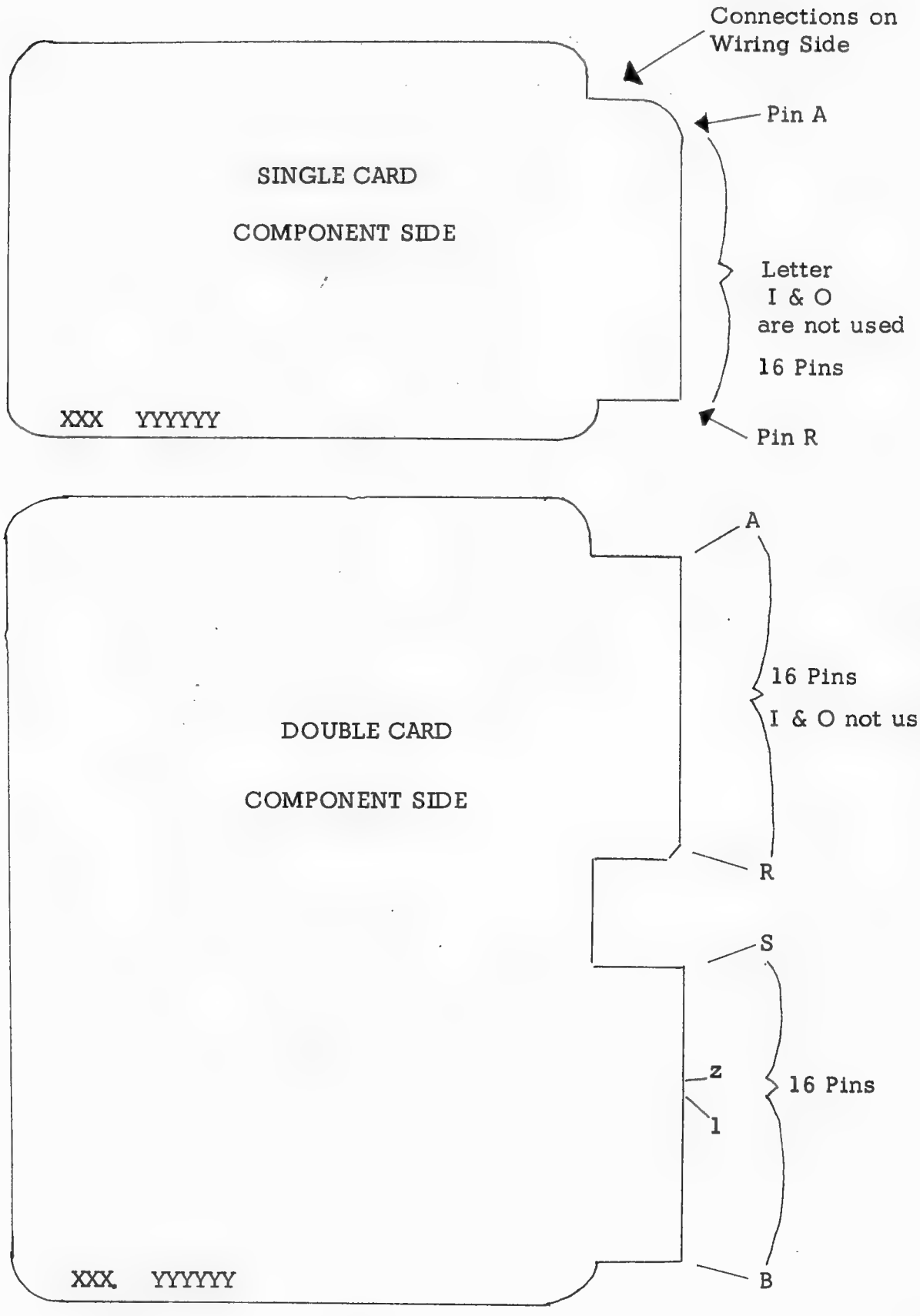


FIGURE 4.27 AKX SMS Card



XXX
2 or 3 Letters
Card Type Code
e.g. MX CAB etc

YYYYYY
6 Digit Part #
e.g. 371661
(MX Card)

PARTS LIST FOR THE BINARY ADDER. — IGNORE

Part Number	Description	Quantity
371661	SMS Card MX	41
371029	SMS Card CD	6
372431	SMS Card AKV	10
451142	Wire Wrap Tool	1
1143198	Lamp 10v 14ma	12
185198	Lamp Holder	12
	Lamp Block	1
	Switch SPDT	20
	Resistor 150 ohm ½w	10
	Resistor 1.6k ohm ½w	45
	Power Supply (complete)	1
	SMS Socket Panel (Part wired)	1
	Wire 24 gauge	AR

SIGNED ASSYNCHRONOUS BINARY ADDER

CHAPTER 5

BASIC DESCRIPTION OF SABA

CHAPTER 5.

BASIC DESCRIPTION OF SABA

The SABA unit is a small transistorized device which can add or subtract two, eight bit binary numbers either or both of which may be negative. The answer may be as big as nine binary bits and is always displayed in true form with an indication light which signifies a negative answer.

The two factors, which we will call A and B, are entered into the unit by two sets of eight, bit switches. The algebraic signs of the factors and also the type of operation (i.e. add or subtract) are set into the unit with switches.

Figure 5.1 is an overall block diagram of the SABA unit. It consists basically of three distinct functional groups of components -

1. The factor assemblers (A & B)
2. The sign control circuits
3. The 8 Bit to 8 Bit adder

The inputs to the factor assembler circuits come from the two sets of bit switches (eight for A and eight for B) and the circuits are further controlled by the sign control circuitry.

The purpose of the sign control circuitry is to analyse the signs of each of the factors and the operation (add or subtract) and then to decide if either one of the factors should be complemented. (An explanation of complement arithmetic will follow later in this chapter).

After the factors have been correctly assembled they are applied to the adder circuitry. This section sums the two sets of input data and handles all necessary carries that may be generated. Attached to the adder is a sign test circuit and an inversion control circuit the purpose of which is as follows:

> When one factor is subtracted from another the answer may be a negative number. If this happens the adder will generate the answer in complement form. The sign test circuit monitors this condition and if it occurs it activitates the negative answer indication and also the inversion circuits which re-complement the number into its true form.
>
> As explained in Chapter one of this manual binary arithmetic is very easily performed manually. It follows all the normal rules of decimal arithmetic. With a machine, however, it is not quite

so easy as it is difficult, although not impossible, to build circuitry which will add and subtract in the same way as we perform this operation manually.

It is much simpler to built a unit which can only add and then to manipulate the input data to achieve the correct result. The method of subtraction used with many machines, including SABA, known as complement addition.

Lets look at an example -

We will subtract binary 01100111 from 10001101, first manually and then in the same way as it will be done by SABA.

Manual Method	10001101	(141 Dec)	Factor A
	01100111	(103 Dec)	Factor B
	00100110	(38 Dec)	Answer
Machine Method	10001101		Factor A
	10011000 +		Complement Factor B
Carry Out	00100101	(37 Dec)	Answer

You will note that the complement is generated by simply turning on those bits which were off and turning off these bits which were on. You will also note that the answer is one less in value than it should be (37 instead of 38) and that a carry out occurred from the high order bit position. If we now take this carry-out and add it back to the units position then the answer will be corrected.

10001101		Factor A
10011000 +		Complement Factor B
00100101	(37 Dec)	Answer
→ 1		
00100110	(38 Dec)	Corrected answer

Let us now sub tract the number 10001101 from 01100111. This will result in a negative answer being generated.

01100111	Fa ctor A
01110010 +	Complement Factor B
11011001	Answer

If we look at this answer it at first appears to be incorrect and also we see that no carry-out of the high order position has occurred. Because the carry did not occur we will not add the one to the units position but we will signal the inversion circuits to operate and the negative answer indication lamp to turn on. All that is performed by the inversion circuits is to complement the answer by turning all ON bits OFF, and all OFF bitsON -

11011001	Answer
00100110 (38)	Inverted answer

Now lets take a closer look at one position of the eight bit adder. (Figure 5.2)

It can be seen that logically it consists of 5 exclusive ORs, 3 ANDS and 1 inclusive OR circuit.

Exclusive ORs number 1 and number 2 are used to generate the complement bits when necessary, under the control of the two signals Comp A and Comp B which are generated by the sign control circuits on Figure 5.1. These two circuits are actually part of the A and B assemblers (Figure 5.1). It will be seen that if the Comp A and B signals are inactive then the output of exclusive ORs 1 & 2 will follow the other input, which comes from the ON output the appropriate bit entry switches. While if the control signals are active then the output of exclusive ORs 1 & 2 requires that the appropriate bit switch be off in order to get an active output. Therefore the input data (from the switches) is effectively inverted or complemented under these conditions.

The output of the circuits 1 and 2 are now exclusively ORed together to provide the partial sum -

E/G,	A $\overline{\vee}$ B	PARTIAL SUM
	0 $\overline{\vee}$ 0	0
	1 $\overline{\vee}$ 0	1
	0 $\overline{\vee}$ 1	1
	1 $\overline{\vee}$ 1	0

This partial sum output of circuit 3 is now exclusively ORed with the carry generated from the previous position to provide the final output or sum. This in turn is exclusively ORed with a control signal generated by the sign test circuits. This signal determines whether the sum will be inverted or not before being applied to the lamp drivers.

We must also check the input bits and the input carry to see if a carry out will be generated to be passed on to the next higher position, e.g.

0 + 1 + CARRY IN	=	0 WITH CARRY OUT
1 + 1 + NO CARRY IN	=	0 WITH CARRY OUT ETC.

This is achieved by ORing together the output of three and circuits one of which will be active if any two of the input conditions are active.

In the case of the highest position this output carry goes to the sign test circuits, where it is ANDed with the minus signals, to be fed back to the low order position, if it is active, or if it is inactive and a subtraction if being performed then is causes the inversion circuits to operate.

On an addition this high order carry is used to turn on the overflow lamp which has a bit value of 256.

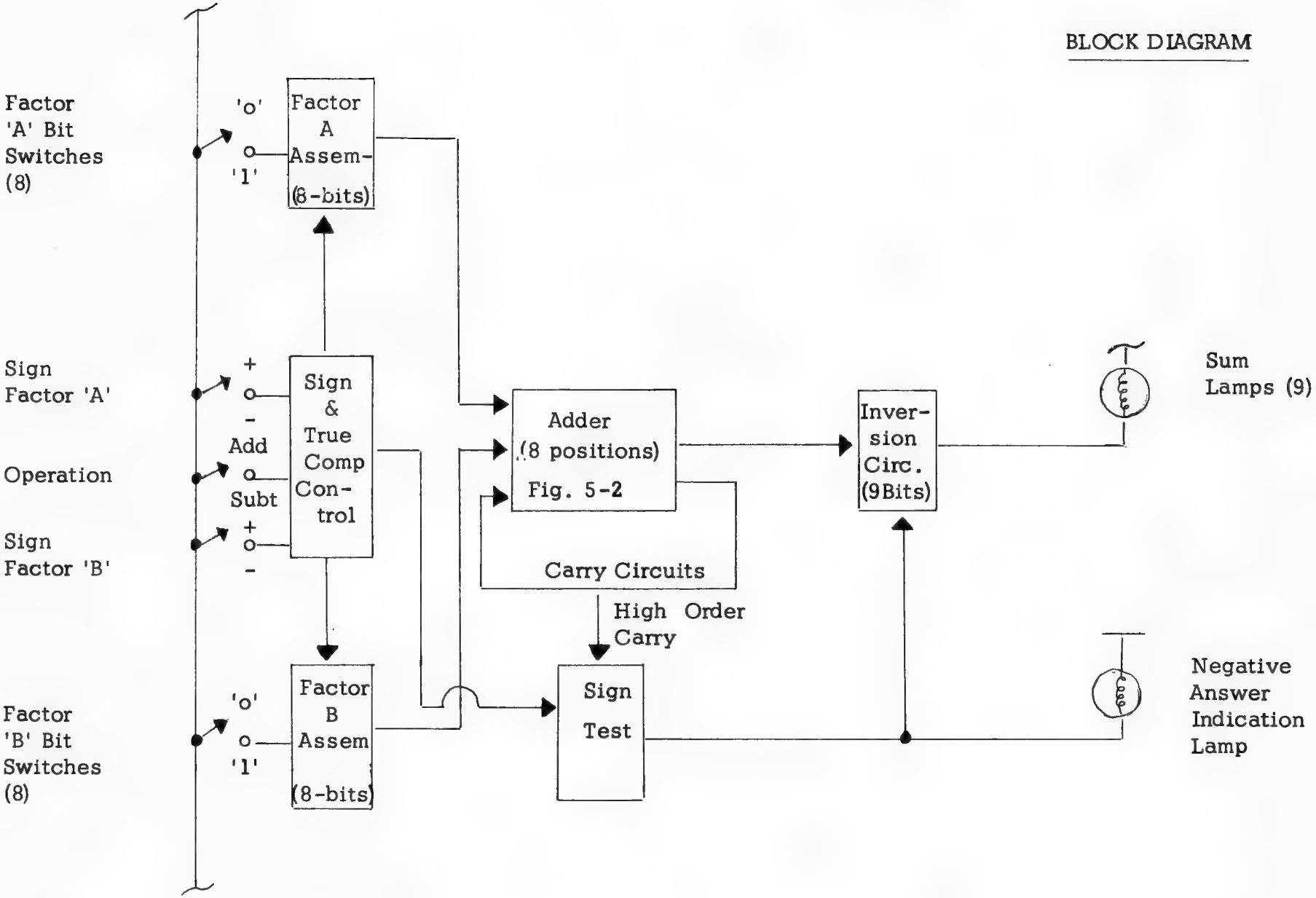
S igned

A ssynchronous

B inary

A dder

BLOCK DIAGRAM



ADDER & BIT ASSEMBLER

1 POSITION

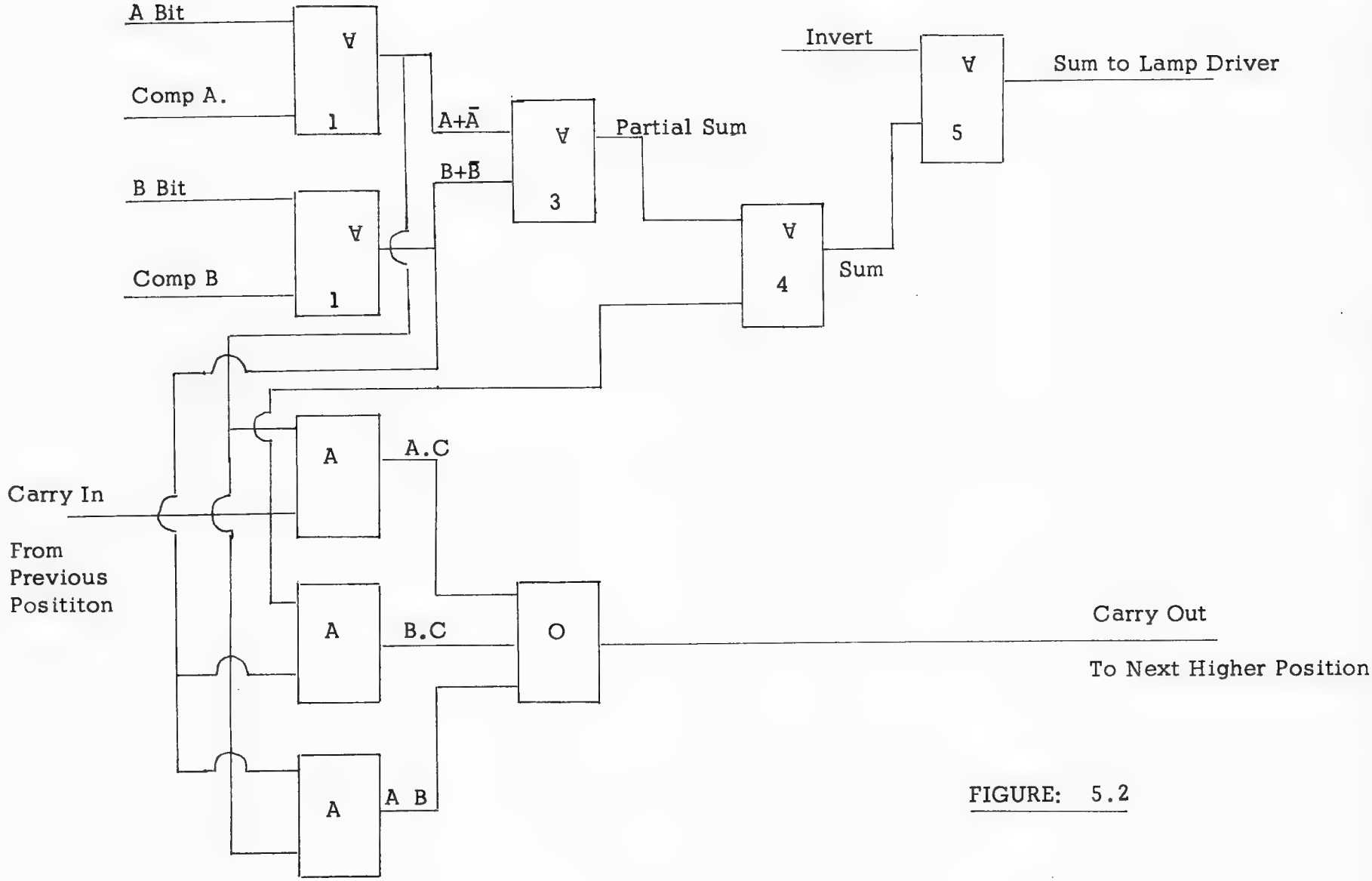


FIGURE: 5.2

SIGNED ASSYNCHRONOUS BINARY ADDER

CHAPTER 6

DETAILED CIRCUIT DESCRIPTION OF SABA

CHAPTER 6.

DETAILED CIRCUIT DESCRIPTION OF SABA

The description which follows is intended to tell you exactly how SABA works, but is not intended to be a point to point wiring guide, the actual construction of SABA and its mechanical layout is left to your own ingenuity.

At the end of this chapter there are eighteen diagrams which, with the exception of the power supply, represents the complete SABA unit.

The first 8 pages (Figures 6.1 to 6.8) are the adder and carry generator circuits, the next 4 (Figures 6.9 to 6.12) are the A factor assemblers, the next 4 (Figures 6.13 to 6.16) are the B factor assemblers and finally the last two pages (Figures 6.17 and 6.18) are the various control circuits which handle sign generation, inversion, etc.

As previous mentioned SABA is a binary adder able to add (or subtract) two eight bit binary numbers with full algebraic sign control. The bit switches for each operand and the output lamps are each numbered, 0 throughout 7, with 0 being the high order bit (decimal value 128) and 7 being the low order bit (decimal value 1). In addition to these there is one extra bit associated with the output, this is the overflow bit and has a decimal value of 256.

The complete SABA design has been built around three basic CTRL card types. A three input AND/OR, a two input AND/OR and an inverter. Sufficient cards of each type are provided in the kit to enable you to build the unit with a minimum of trouble.

Lets now have a look at one position of the adder and find out how really it works. As each position is identical we will concentrate on position 4 Figure 6.5, as an example.

Each of the pages 6.1 through to 6.8 may be divided into two parts. The upper half of the page is the adder while the lower half is the carry generator.

Looking at the upper half of page 6.5, on the left hand side we find two 2 input nor circuits used as ANDS. Rember that only when the two inputs are (O volts) at the same time will the output be - (-12 volts). These two AND circuits feed into another 2 input nor used this time as A- OR, i.e. whenever either or both of the inputs are negative (-12 volts) the output is positive (O volts). These three circuit blocks form an exclusive OR, now lets have a look at the inputs to the two ANDS.

The upper AND has factor A bit 4 (from the bit assembler, to be discussed later) applied to it on the upper input and not factor B bit 4 to its lower input. This means that this and black will operate when the factor A bit 4 switch is on and the factor B bit 4 switch is off. If neither switch is on or if both are on then this block cannot function.

The lower of the two ANDs has the opposite condition applied to it. It will operate if factor B switch 4 is on and factor A switch 4 is off. Again if both are on or both are off the AND will not function. The outputs of these two ANDs are ORed together in the following 2 input nor block to give a positive output if factor A switch is on by itself or if factor B switch 4 is on by itself. Again if both are on or both are off then the output of this OR block is negative (-12 volts).

These three circuit blocks therefore have effectively summed together bit 4 of the two factors -

A BIT 4	B BIT 4	OUTPUT OF OR	
OFF	OFF	-12 VOLTS	0 + 0 = 0
OFF	ON	0 VOLTS	0 + 1 = 1
ON	OFF	0 VOLTS	1 + 0 = 1
ON	ON	-12 VOLTS	1 + 1 = 0

The output of this OR is taken to two different circuit blocks, directly to another AND and also through an invertor to yet another AND. Remember, the output of the invertor is exactly opposite to its input, if the input is 0 volts (+). Then the output is -12 volts (-) and visa versa.

These two new ANDs and the OR which follows them form another exclusive OR which operates in an identical manner to the first set of circuits, i.e. only with one of the input signals active will there be a final output.

Lets have a look at the inputs to these new ANDs. One input comes from the previous exclusive OR, if this is positive (0 volts) then the lower input of the upper AND will be conditioned, if it is negative (-12 volts) then the action of the inverter will condition the upper input of the lower AND.

The lower input of the lower AND is conditioned if a carry was received from the previous position of the adder (in this case bit 5) and the upper

input of the top AND is conditioned if bit 5 did not generate a carry. This means then that these two ANDs again have exactly opposite inputs.

In other words, we are now adding a possible carry to our previous partial sum to develop the actual sum of the three possible inputs (factor A, bit 4, factor B, bit 4 and a possible carry from bit 5).

A BIT 4	B BIT 4	CARRY FROM BIT 5	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	0	0
0	0	1	1
0	1	1	0
1	0	1	0
1	1	1	1

At this point we now have the final sum for this position of the adder and all we really have to do is to use it to turn on a lamp. However, the control circuits, yet to be discussed, may have detected that this is a negative answer (i.e. one in complement form) and therefore it should be inverted. In order to accomplish this the sum signal is passed through one more exclusive OR, exactly similar to the previous ones. Here it is ORed with the signal Invert which is generated by the control circuits. This causes the lamp to light whenever the sum is 0 (-12 volts) if invert is active or whenever the sum is 1 (0 volts) if invert is not active.

The final output of the last two input NOR is used to drive a lamp to indicate whether the bit is active or not. You will note from Figure 6.5 that this circuit does not have an internal collector load resistor to the -12 volt supply, instead the load consists of the two external resistors and the 10 volt, 14 milliamp lamp.

The reason for the resistors is as follows; the 150 ohm series resistor is to reduce the voltage on the lamp to 10 volts when the transistor is turned on and also to reduce the surge current through both the lamp and resistor at the instant of turn on. This surge is due to the fact that the resistance of a cold tungston lamp may be only about one twentieth of the hot resistance. To further reduce this effect the 1.6K ohm resistor to ground bleeds a small amount of current through the lamp all the time. This current is not sufficient to cause any visible light output from the lamp but it does keep the filament 'warm' and therefore

reduces the resistance change when the lamp is switched on and hence reduces the current surge which if not reduced, may cause premature failure of the lamp and of the transistor which drives it.

Now that we know how the adder operates lets take a look at the carry generator.

The carry generator is necessary to analyse the three possible input bits and to transmit a new carry to the next higher bit position is required.

The conditions which will cause a carry to be generated are as follows:

A BIT 4	B BIT 4	CARRY FROM BIT 5	SUM	CARRY OUT BIT 4
0	1	1	0	1
1	1	0	0	1
1	0	1	0	1
1	1	1	1	1

As can be seen from the above table, if two or more of the three possible bits are active then a carry must be generated for use in the next higher position of the adder.

The circuit to do this is very simple, consisting of three 2 input NOR blocks used as + ANDs, one 3 input NOR used as A - OR and one inverter. Each AND is conditioned with two of the three possible inputs. For example, the upper AND will be conditioned if Factor A bit 4 and Factor B bit 4 are both on at the same time. The second AND with Factor B bit 4 and a carry in from bit 5 and the last with Factor A bit 4 and a carry in from bit 5. If one or more of these ANDS operates the output of the following or becomes (0 volts) and the carry out is sent to the next higher bit position as the carry in from bit 4. Conversely if none of the three ANDs are active then the output of the inverter becomes active and the not carry line to the next position is conditioned.

Now lets take a look at the bit assembler on Figures 6.9 to 6.16. We will use Figure 6.11 which contains the circuitry for Factor A bits 4 and 5. Bit 4 is the upper half of the page and bit 5 is the lower half. All other bit positions including the factor B bits are similar to Figure 6.11.

Again the important circuit is an exclusive OR made with two 2 input ANDS and one two input -OR. The ANDs are conditioned by a control signal called Comp A or not Comp A, which is generated by the control circuits. The other input of each AND comes directly from the bit switch itself.

If the switch is on (logical 1 position) then the lower input of the upper AND has 0 volts (+) applied and the upper input of the lower AND has -12 volts (-) applied via the 1.6K ohm resistor. If the switch is off the conditions are reversed.

The complement control signal governs whether the on or the off condition of the switch with condition the output of the OR to a (0 volt) level. The invertor is used to generate A + (0 volt) level when the output of the OR is - (-12 volts). These two signals are the ones used as Factor A inputs with the adder bit position 4 which we have already discussed.

All other A bits are identical with bit 4, and the only difference with the Factor B bits is the use of a signal called Comp B or Not Comp B instead of the Comp A or not Comp A signals.

The Comp control signals are generated by the control circuits when either one of the factors must be complemented to allow a subtraction (complement add) to be performed.

The control circuits, which we will now discuss are the heart of the machine and are logically the most difficult section to understand. They occupy two pages. Figures 6.17 and 6.18, and in most cases we will have to take both pages together.

These circuits enable SABA to handle all possible variations in the equation.

$$(\pm A) \quad \pm(+B) \quad = \quad (\pm C)$$

and also to make sure that a negative answer is always displayed in true form with a sign indication.

Figure 6.18 contains the circuitry to generate the Comp A and Comp B signals which are used with the factor assemblers already discussed. These signals allow either one or the other of the two factors to be complemented but not both at the same time.

1.	(+A) + (+B) = (+C)	Neither Factor complemented
2.	(+A) - (+B) = ($\pm$C)	Factor B complemented
3.	(-A) + (+B) = ($\pm$C)	Factor A complemented
4.	(-A) + (-B) = (-C)	Neither Factor complemented
5.	(-A) - (+B) = (-C)	Neither Factor complemented
6.	(+A) - (-B) = (+C)	Neither Factor comple mented
7.	(-A) - (-B) = ($\pm$C)	Factor A complemented
8.	(+A) + (-B) = ($\pm$C)	Factor B complemented

The table above shows the conditions under which the two factors need to be complemented.

If we first refer to Figure 6.17 we will find, at the top of the page, that the signals add and subtract are generated directly from a single pole double throw switch and that these signals are used on Figure 6.18. On Figure 6.18 we will find the two switches which set the signs of the two factors. At the top left is a single pole switch which sets the sign of Factor A, only one output is needed here, that for a negative sign. Lower down on the left hand side is the B Factor sign switch. This switch generates output for both a positive and a negative sign.

Before we start to analyse the actual circuit. A word about the two groups of inverters in the Comp A and Comp B outputs will not go astray.

The Comp A signal is generated whenever the AND circuit labled 1* is satisfied. The output of this AND is negative (-12 volts) and therefore the first inverter is needed to make this a Comp A signal. If the 1* AND is not active then its output is (0 volts) and the not Comp A signal is generated. The remaining two inverters associated with this circuit have no logical purpose, this is also true of the last two inverters following the Comp B and 2*. They are necessary because any one of these CTRL circuits can only drive approximately six new circuits and these signals go to more than six places. By including the extra invertors we can drive a number of circuits from the original signals and an additional group from these extra outputs without overloading any one circuit. You will notice that there are two Comp A lines, two Comp B lines and also two lines for each of the Not Comp Signals, and also that these are labled Net 1 and Net 2. When you build the machine make sure that you connect the appropriate nets to the circuits as shown in the various pages of the diagrams.

Now back to the logic, if we again examine the table above we will find that it actually reduces to four operations. Line 1 equals line 6 mathematically. Line 2 equals line 8, line 3 equals line 7 and line 4 equals line 5. This simplifies our job considerably so lets see how the circuiting handles lines 1 through line 4.

Line 1

The sign of Factor A switch would be in the position which means that AND A 1* has a negative (-12 volts) applied to its upper input. This in turn causes the output to be (0 volts) so that the signal Not Comp A is active. If you now go back to (say) Figure 6.11 you will find that the A assembler Bit 4 outputs (and in fact all the other A bits) will now become active when their associated bit switches are on.

Line 1 (continued)

The sign of Factor B switch would also be in the + position however neither of the two ANDs associated with this switch can operate. The upper one can't because the sign switch is + and the lower one can't because we are not subtracting (Figure 6.17). If you now follow the levels through you will find that this results in the Not Comp B signals being active (0 Volts) and therefore the on state of the Factor B switches will be used in the B assembler diagrams.

Line 2 and Line 3

Why don't you follow the rules and work these two cases out for yourselves.

Line 4.

Because both factors are negative we don't need to complement either of them if we add them together and insure the negative answer indicator is turned on then everything will be correct. This is accomplished by conditioning the AND circuit 3* because A is negative, B is negative and the operation;is an add. When AND 3* is conditioned its output goes to -12 volts which prevents the ANDs 1* and 2* from being conditioned. Therefore neither factor A nor Factor B is complemented.

Why don't you apply the rules and work out the rest of the examples for yourselves.

Now that we have analysed the operation of the factor assembler controls (Figure 6.18), lets turn to Figure 6.17 and look into these circuits.

Looking again at the previous table you will see that whenever only one of the factors is to be complemented the operation will be a mathematical subtract but that if neither are to be complemented the operation is a mathematical add. This is an exclusive or function.

Near the top of Figure 6.17 you will find an exclusive OR made up of the usual three, 2 input, NOR circuits. The output of this will be positive (0 Volts) when either one of the factors is to be complemented if neither are to be complemented (or both) then the output is negative (-12 volts). This circuit generates two new signals called minus (A or B Comp) and plus (neither A or B Comp).

Further analysis of the Table will show that Lines 1 and 6 always result in a positive answer. That Lines 4 and 5 always result in a negative answer and in the other four cases the answer could be either positive or negative.

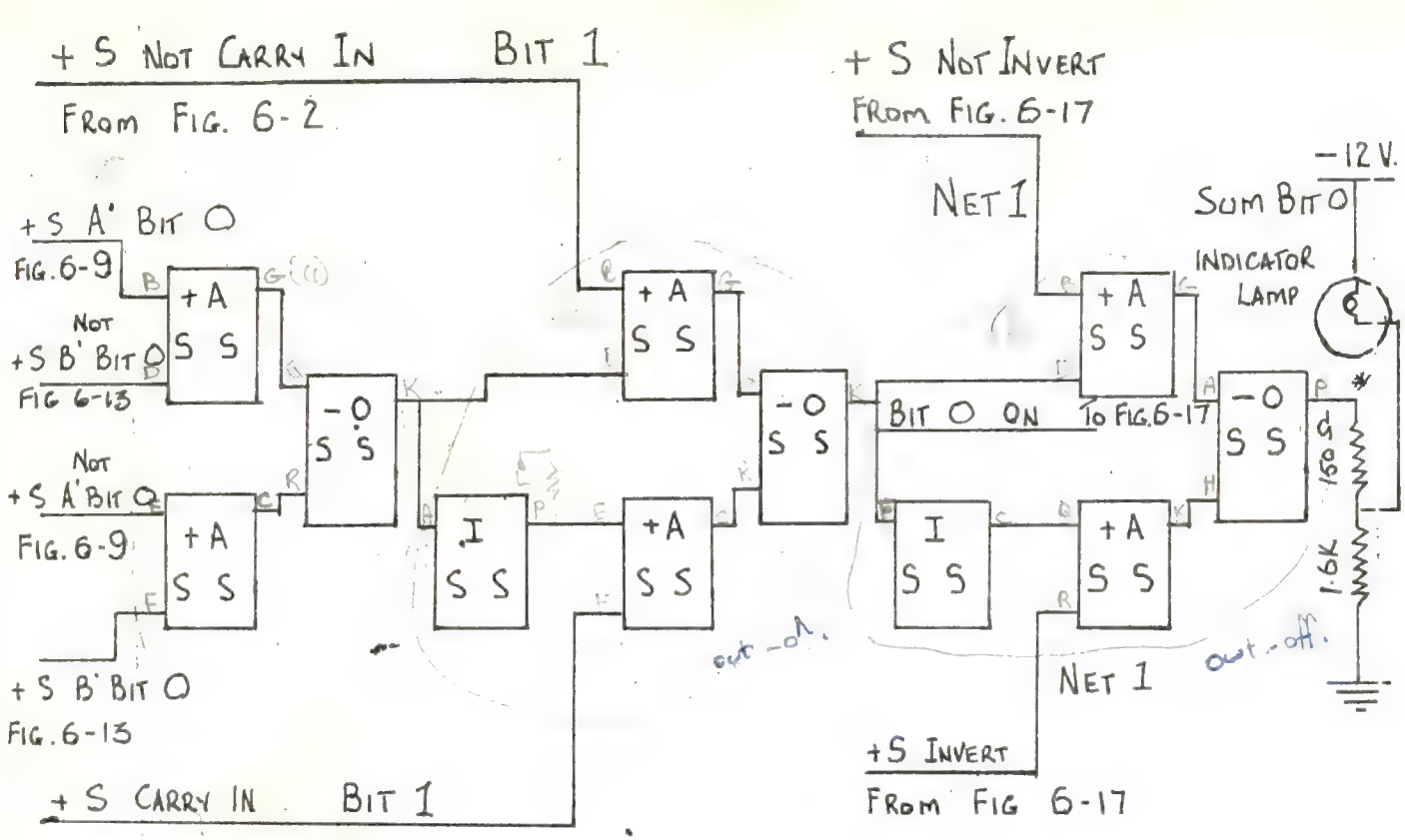
Lets see how we turn on the negative answer lamp for lines 4 and 5. As can be seen from Figure 6.18 both of these conditions result in conditioning the AND 3*. The negative output of this AND prevents complementing either factor and also comes across into Figure 6.17 as the lower input to the -OR which drives the negative sign lamp. This signal causes the lamp to be turned on.

You will remember from Chapter 5 that when we subtract a large number from a smaller number the answer will be in complement form and must be inverted for it to be meaningful. You will also remember that whenever this happened the high order position of the adder (bit 0) did not generate a carry-out. Lets utilize this lack of a carry out to activate the invert and the lamp circuits. AND 4* is conditioned if minus is active and there is no carry from bit 0. It will immediately bring the line invert to an active level which will allow the adder to re-complement the answer (Figure 6.5). Also this invert signal ANDed with A + (0 Volt) level from the eight input dot AND will turn on the lamp. The reason for the eight input AND is in case the two factors were exactly equal when a subtraction is performed. Under these conditions all bits would be on. The no Bit 0 carry would cause an inversion of the answer to an all off indication but the negative lamp will not be turned on (a negative zero answer would be confusing).

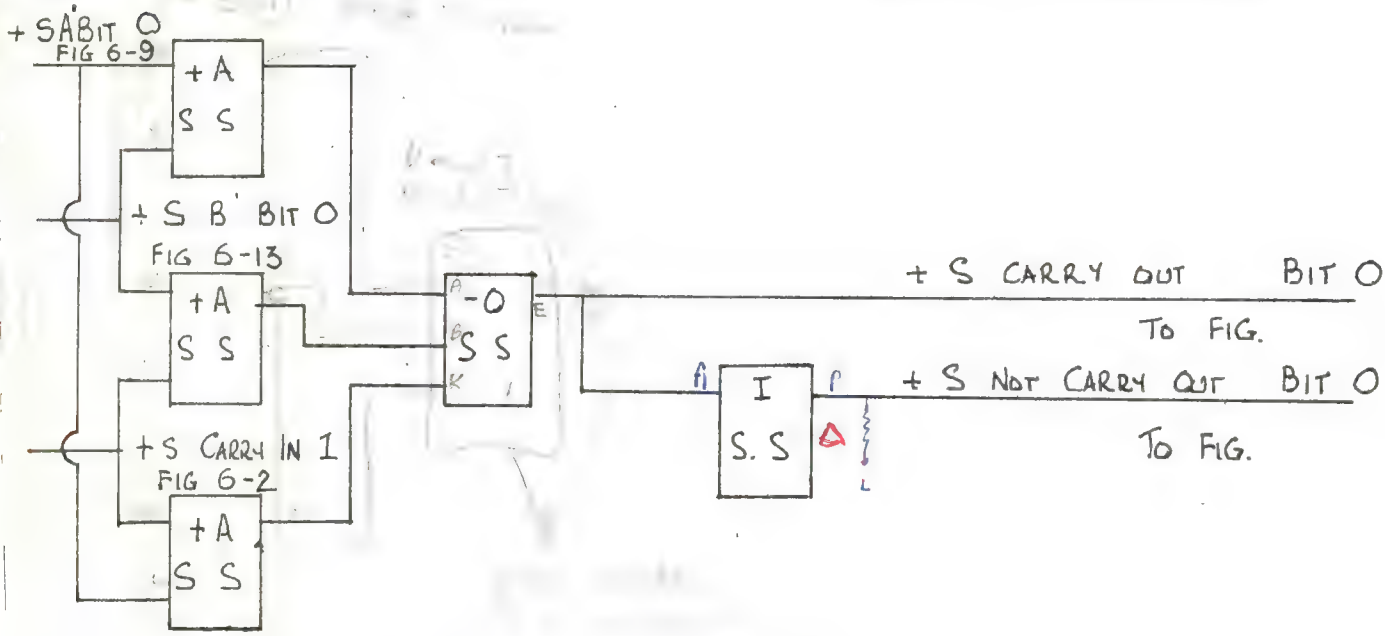
The remaining two circuits on this page are extremely simple.

One is used on a subtraction operation to add a carry-out of bit 0 position back into the carry-in of bit 7 to correct the answer. The other detects a carry out of Bit 0 of the adder during an add operation and turns on the overflow lamp which has a bit value of 256.

Well now you know all about SABA and when you have read the section on suitable power supplies you will be able to build one of your own.



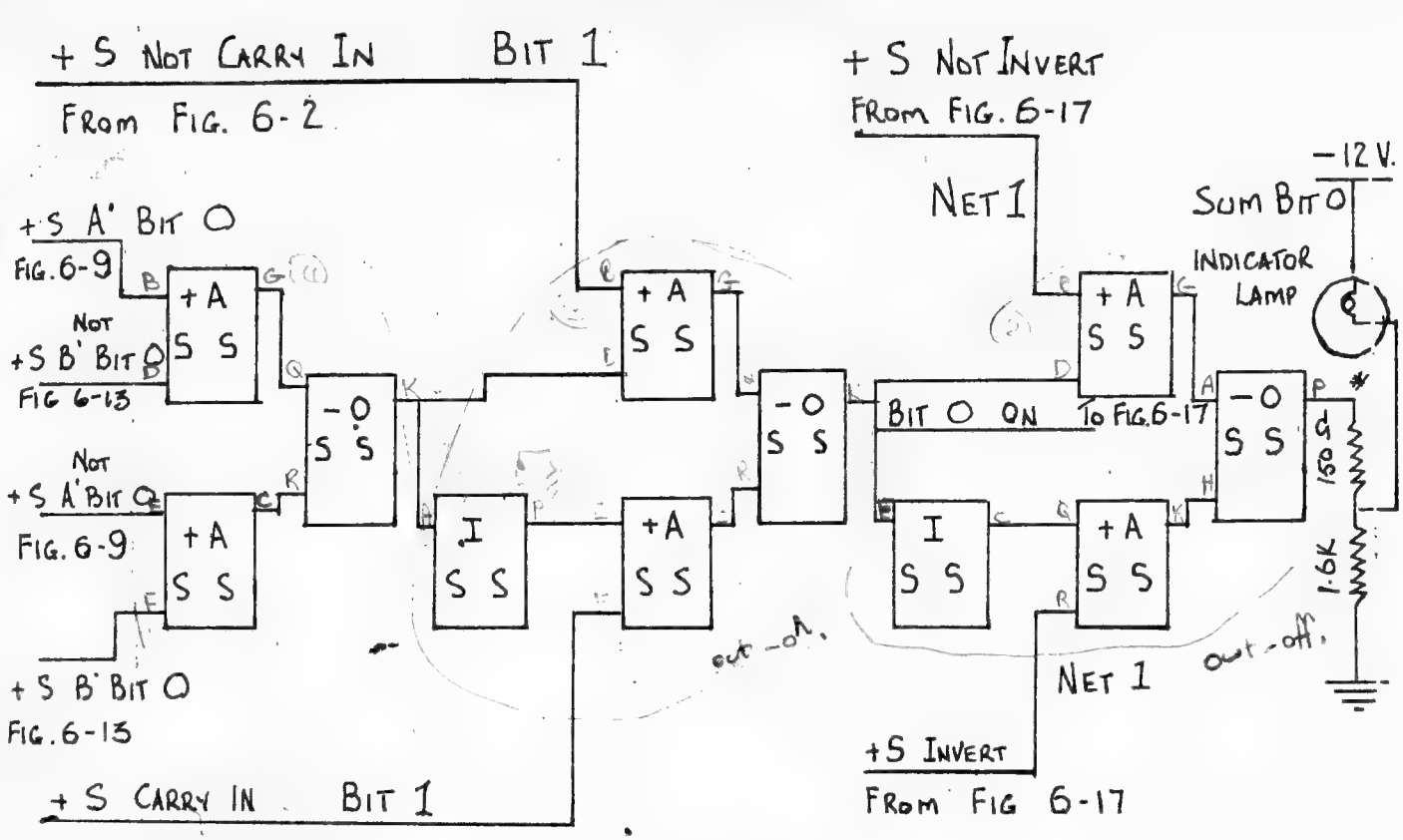
* THIS CIRCUIT DOES NOT HAVE A LOAD RESISTOR



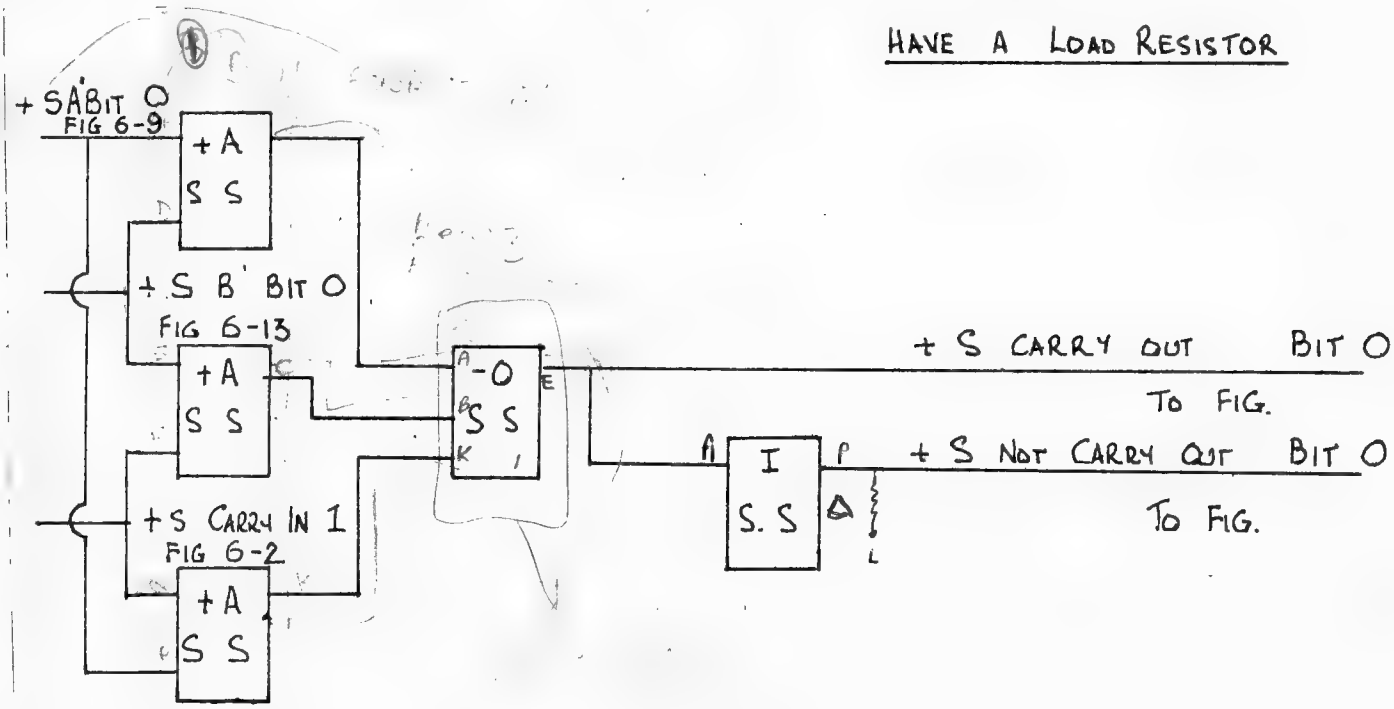
ADDER & CARRY GENERATOR

BIT POSITION O

Fig: 6 - 1



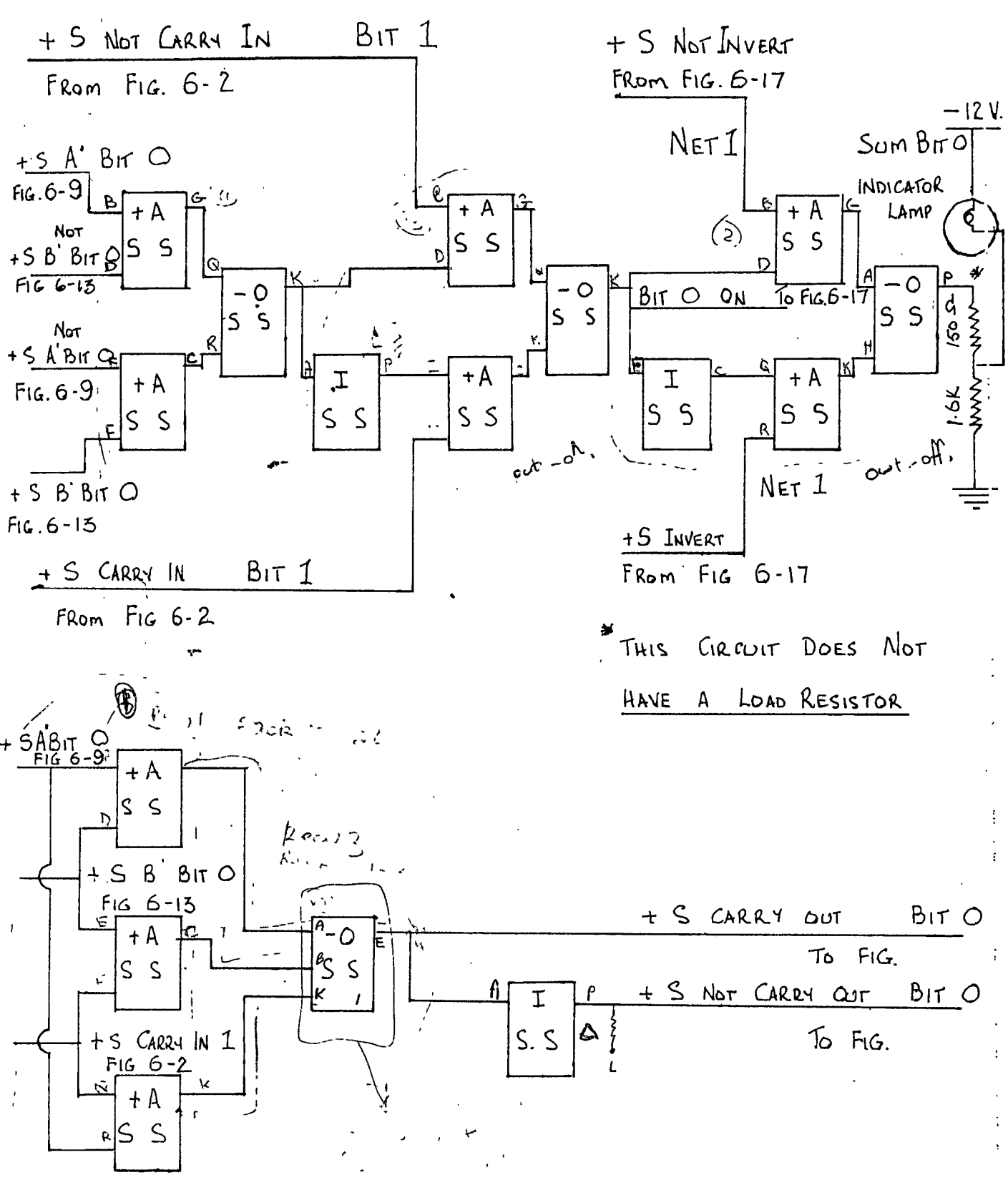
* THIS CIRCUIT DOES NOT HAVE A LOAD RESISTOR



ADDER & CARRY GENERATOR

BIT POSITION O

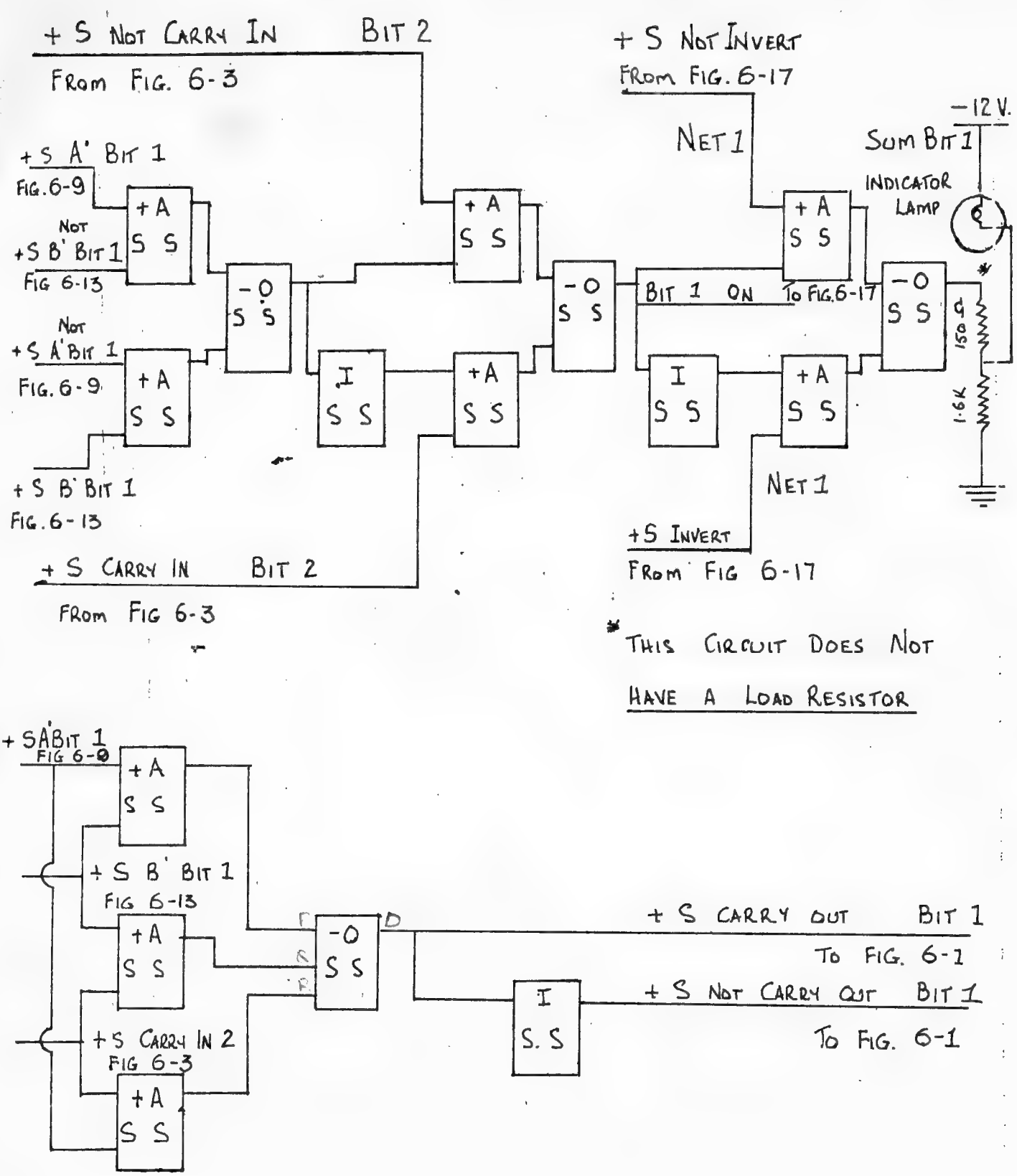
Fig:6-1



ADDER & CARRY GENERATOR

BIT POSITION O

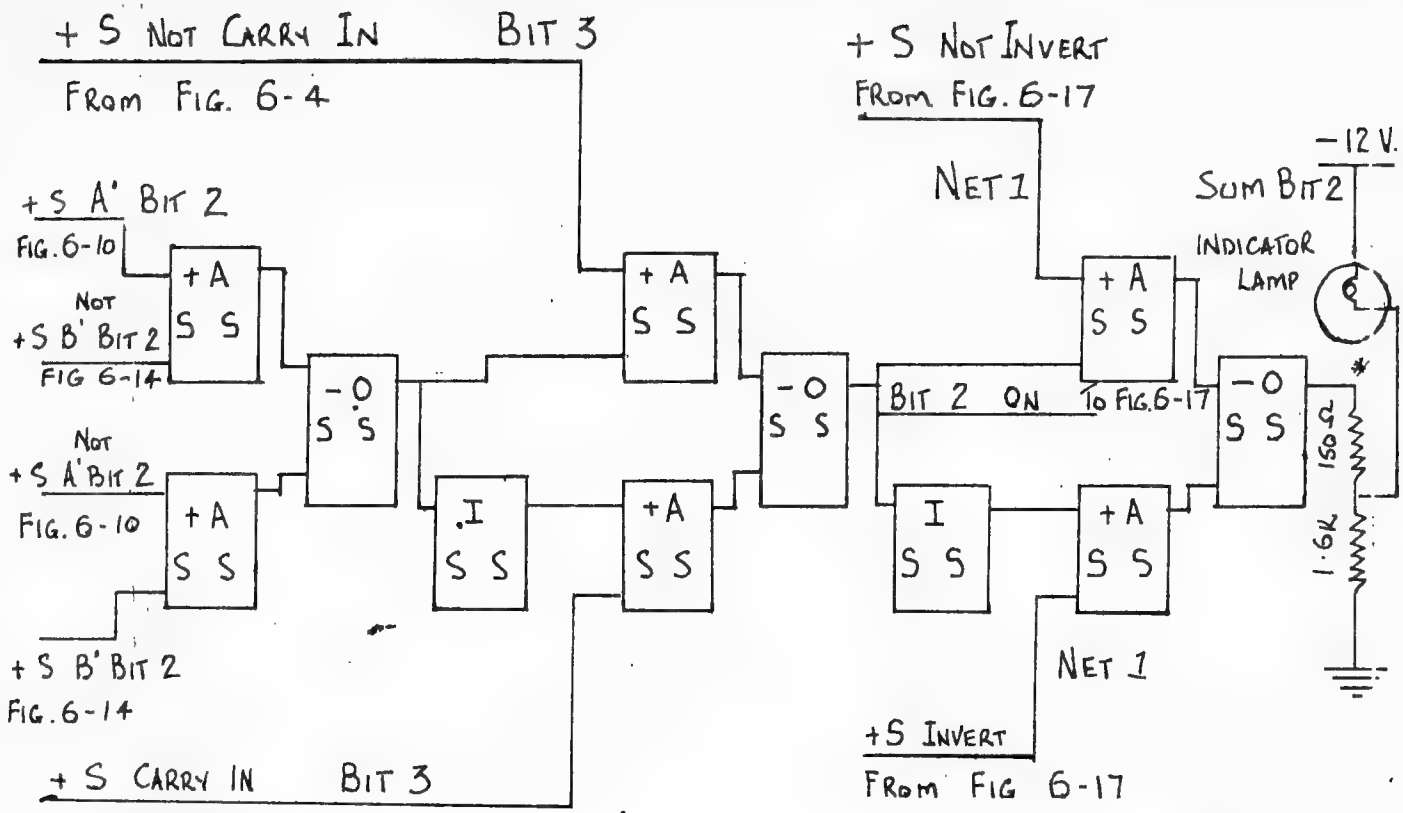
Fig: 6 · 1



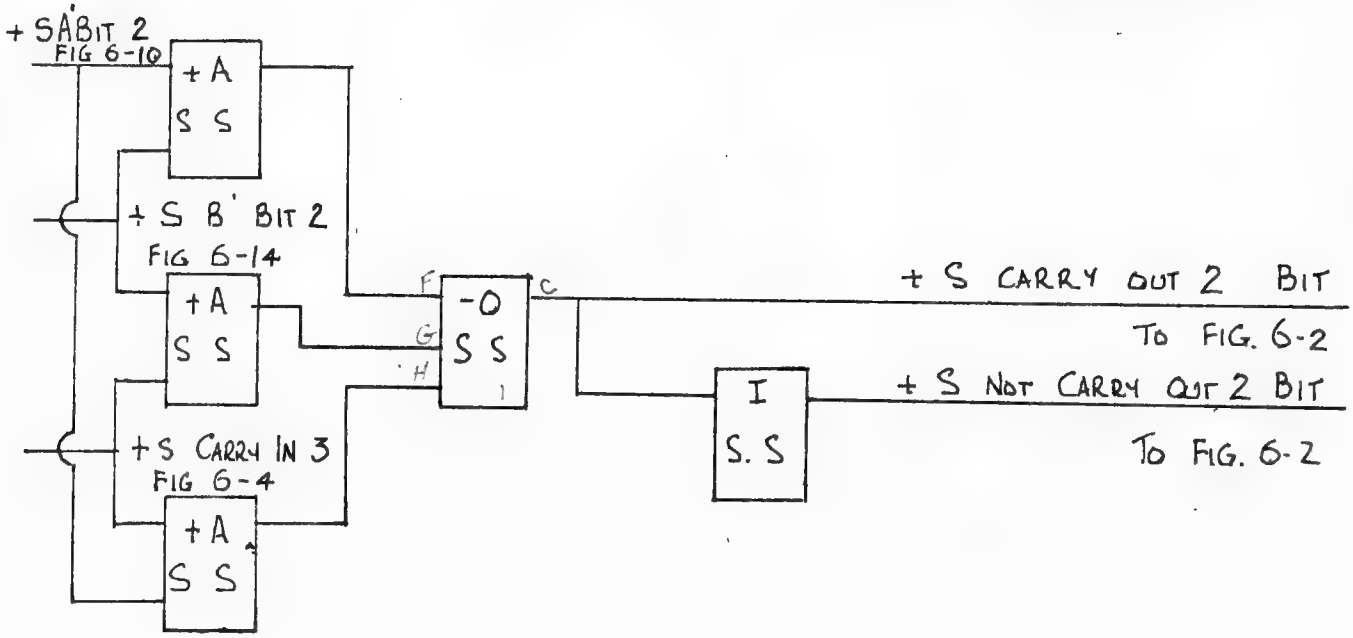
ADDER & CARRY GENERATOR

BIT POSITION 1

Fig:6-2



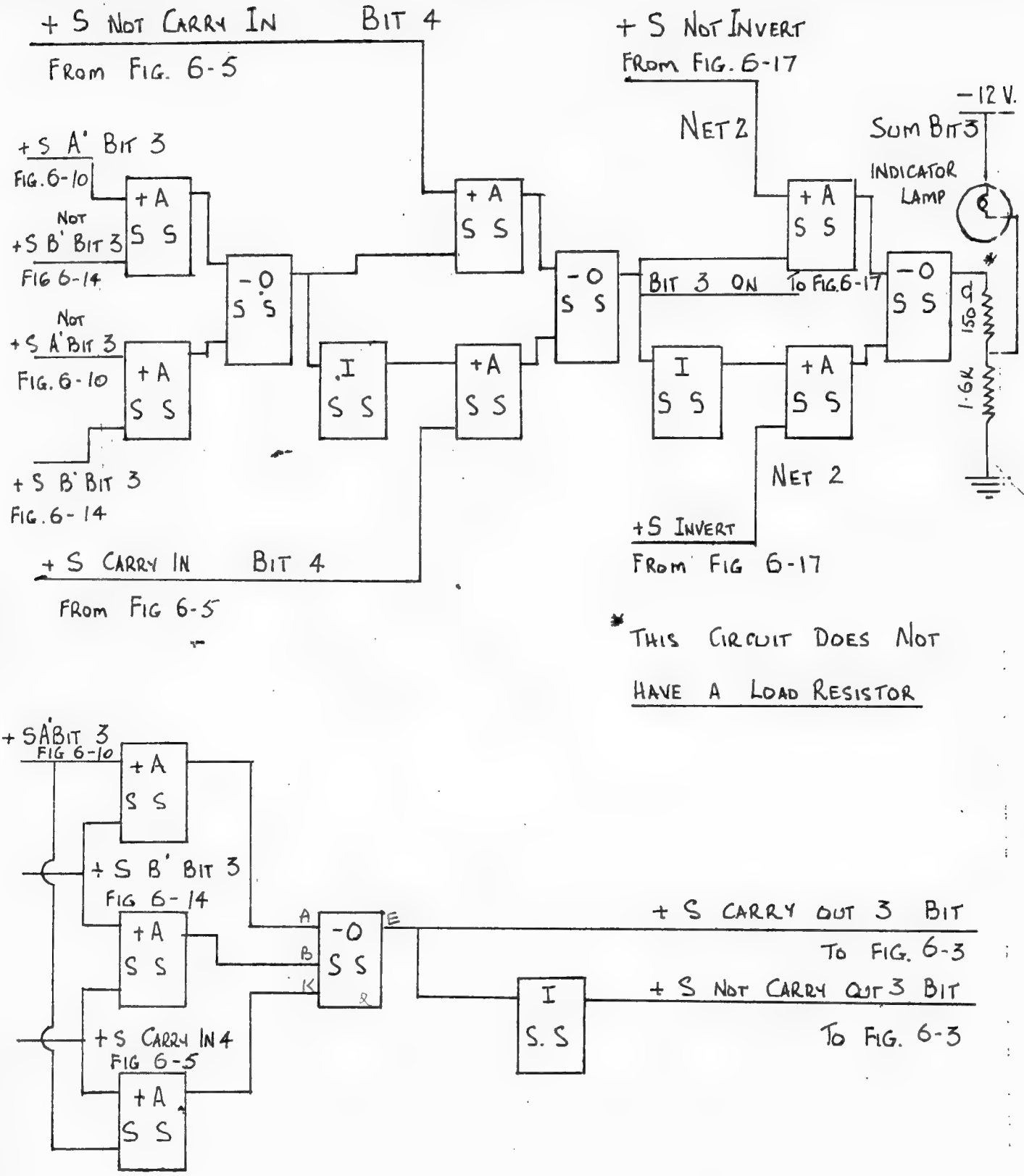
THIS CIRCUIT DOES NOT HAVE A LOAD RESISTOR



ADDER & CARRY GENERATOR

BIT POSITION 2

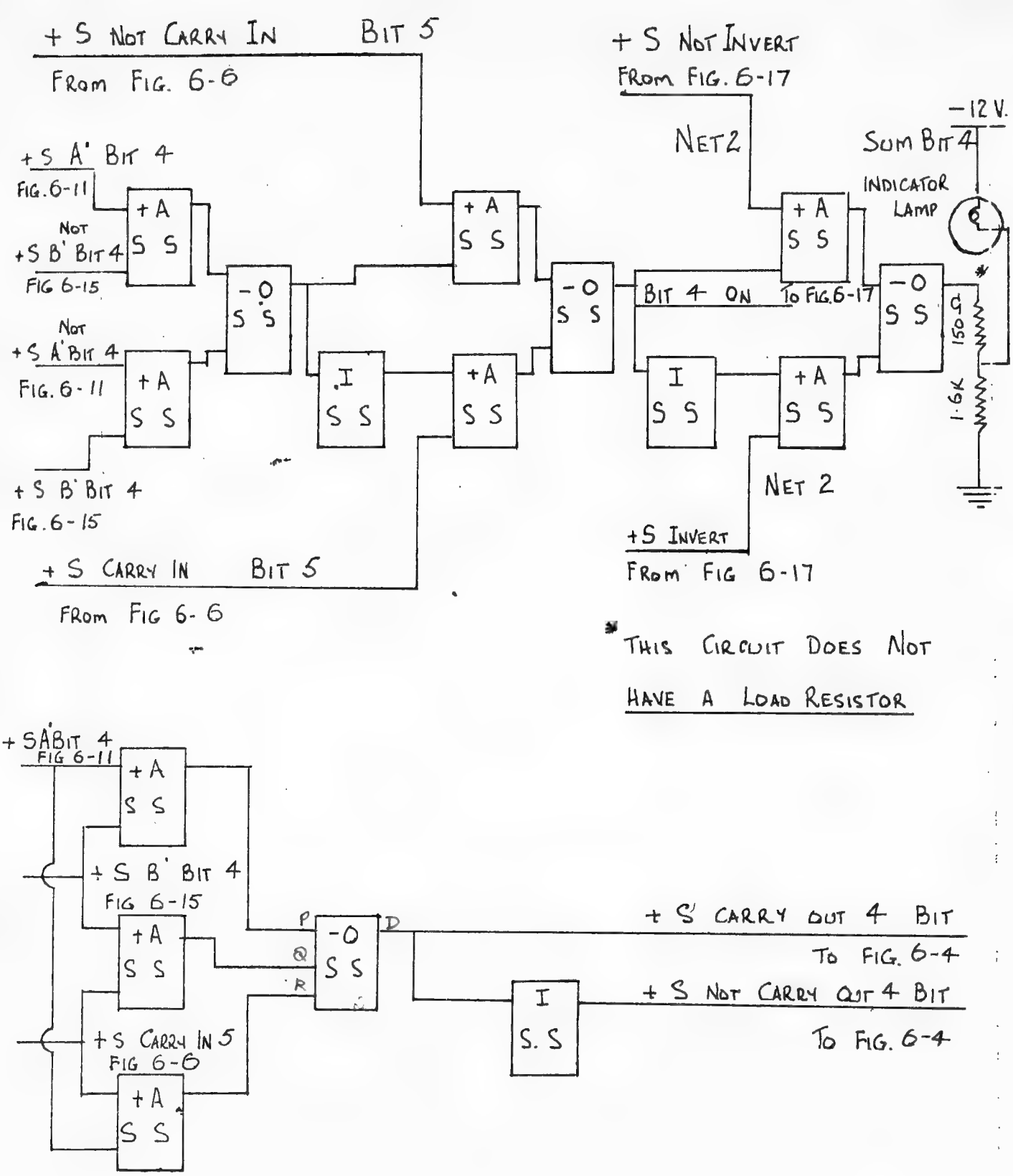
Fig:6-3



ADDER & CARRY GENERATOR

BIT POSITION 3

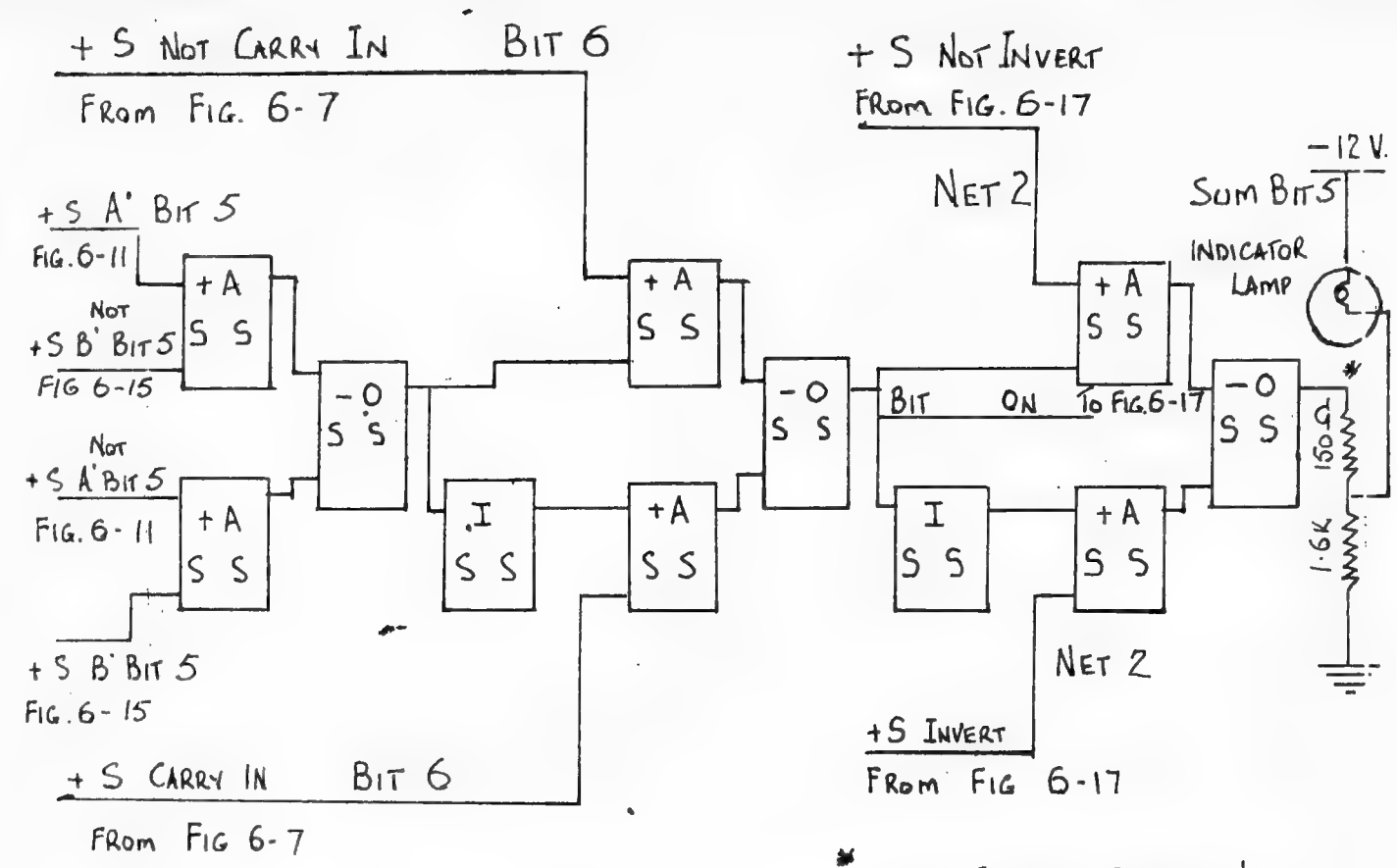
Fig:6- 4



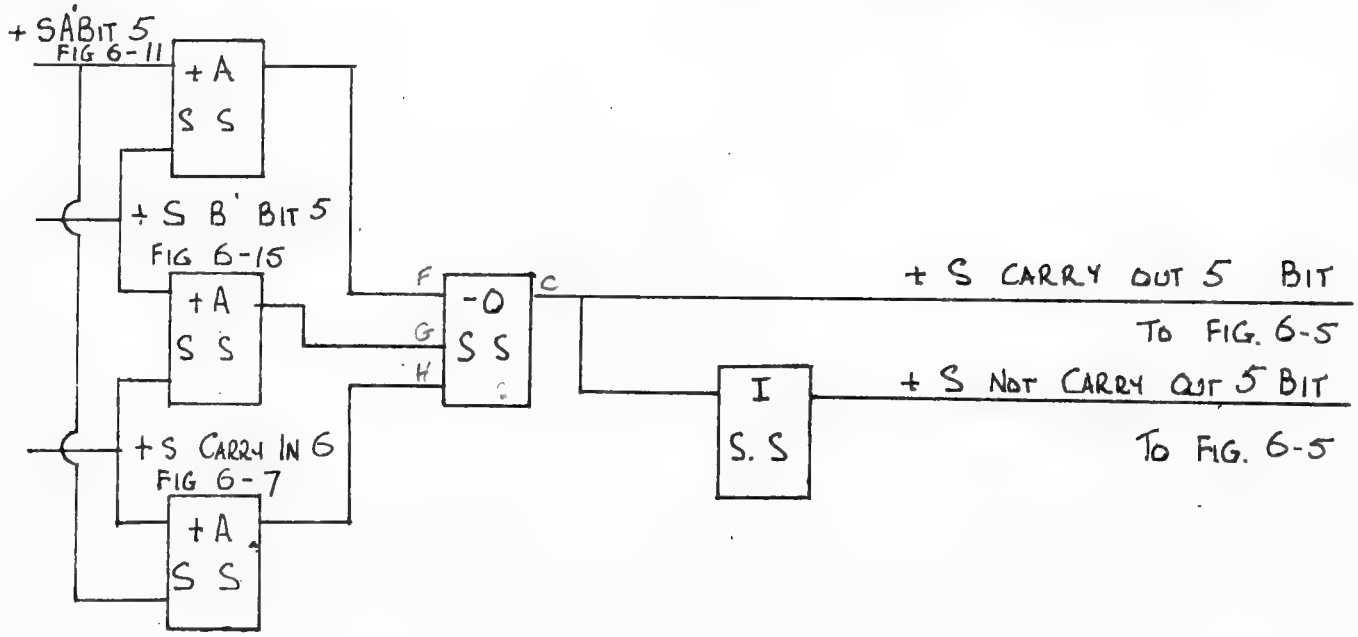
ADDER & CARRY GENERATOR

BIT POSITION 4

Fig: 6-5



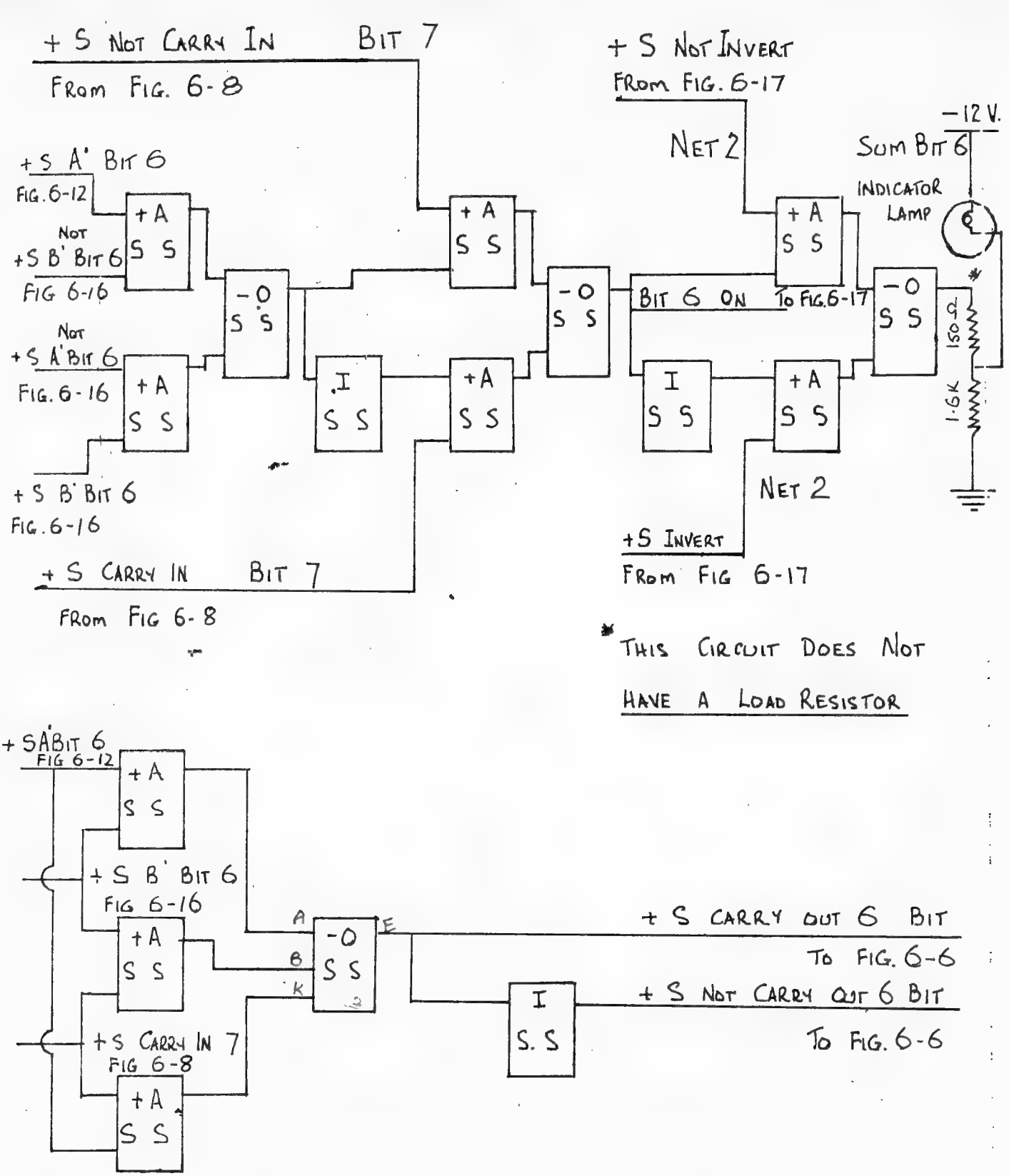
* THIS CIRCUIT DOES NOT HAVE A LOAD RESISTOR



ADDER & CARRY GENERATOR

BIT POSITION 5

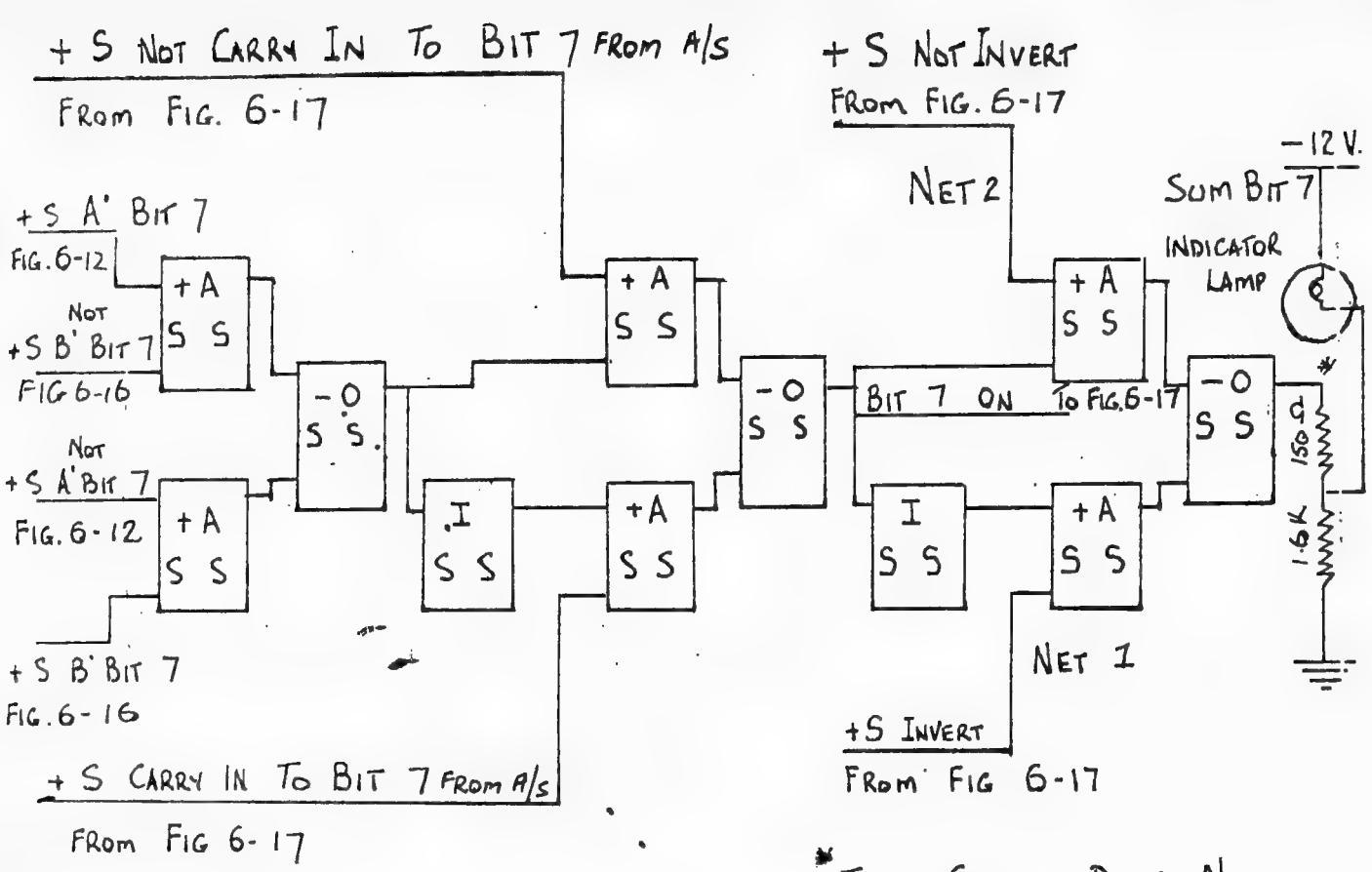
Fig: 6 - 6



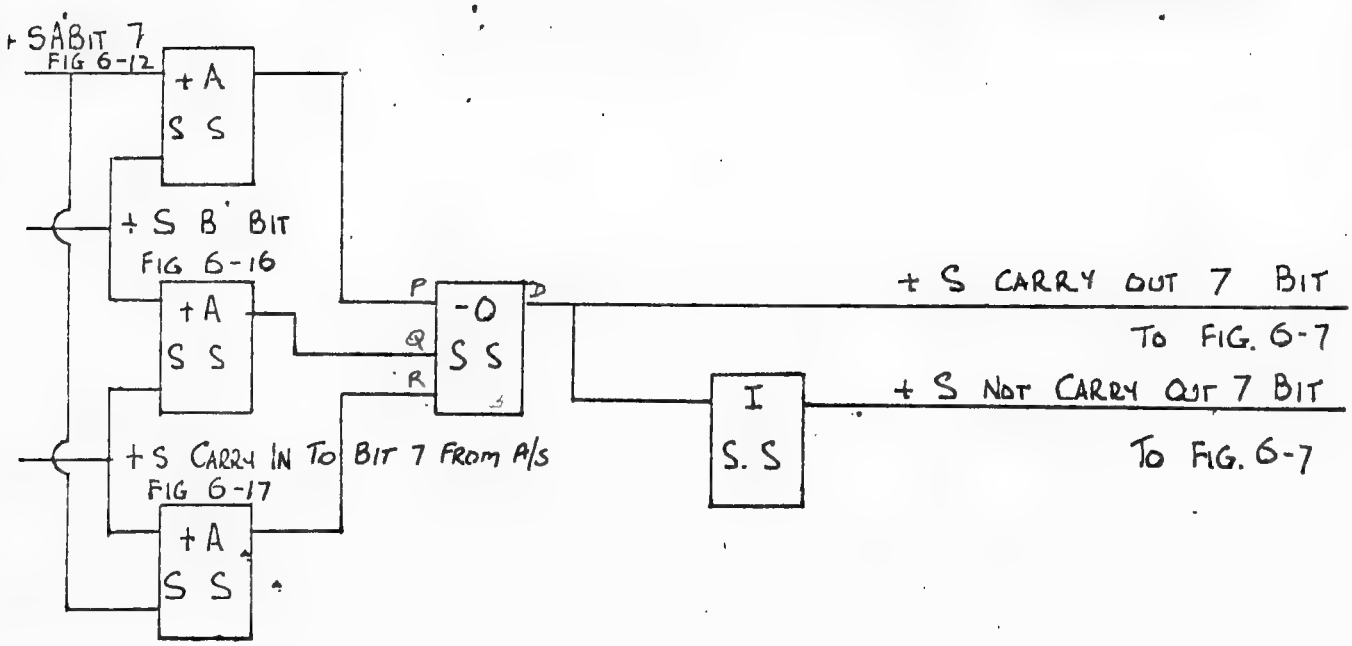
ADDER & CARRY GENERATOR

BIT POSITION 6

Fig:6-7



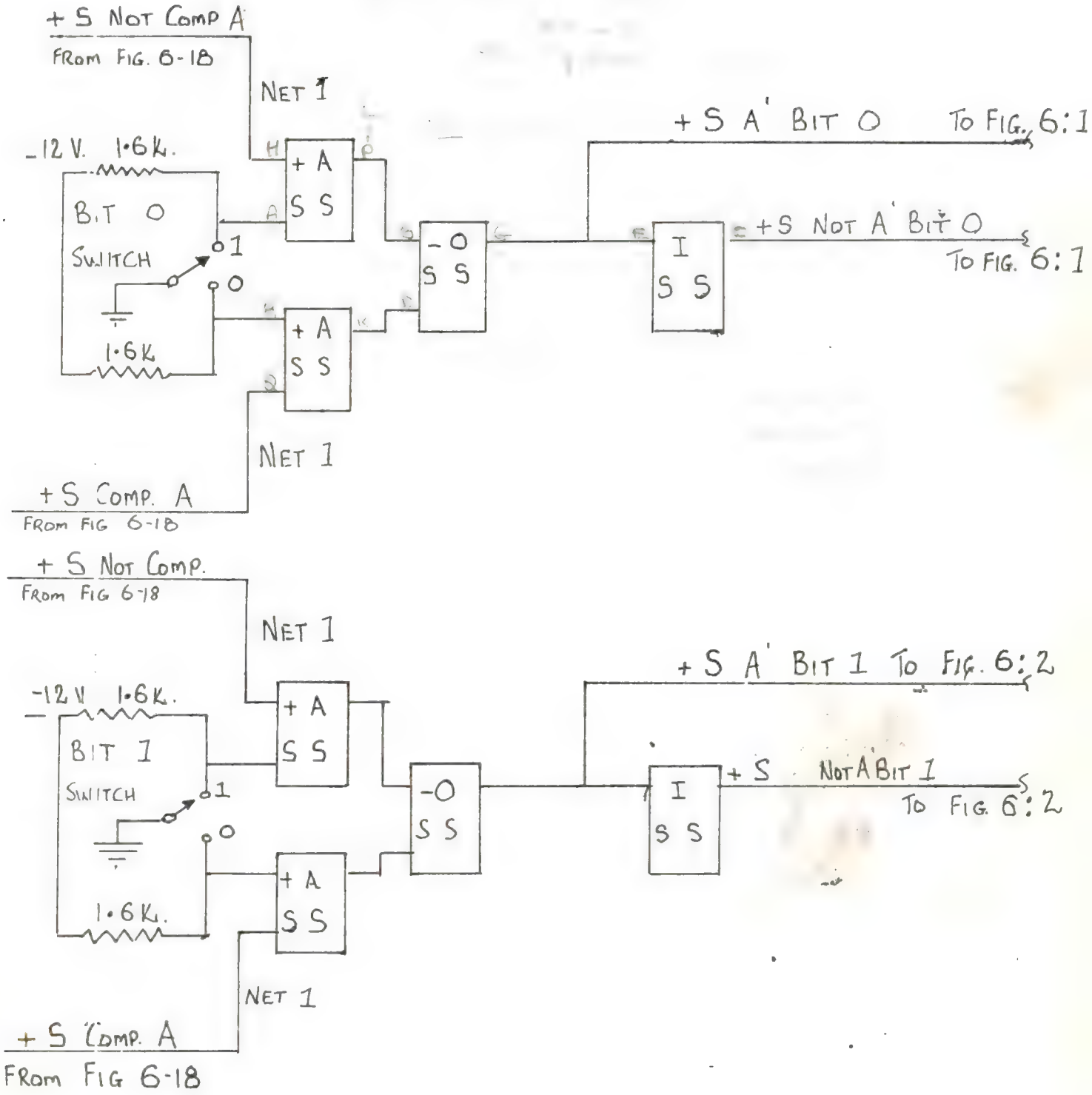
* THIS CIRCUIT DOES NOT HAVE A LOAD RESISTOR



ADDER & CARRY GENERATOR

BIT POSITION 7

Fig:6·8

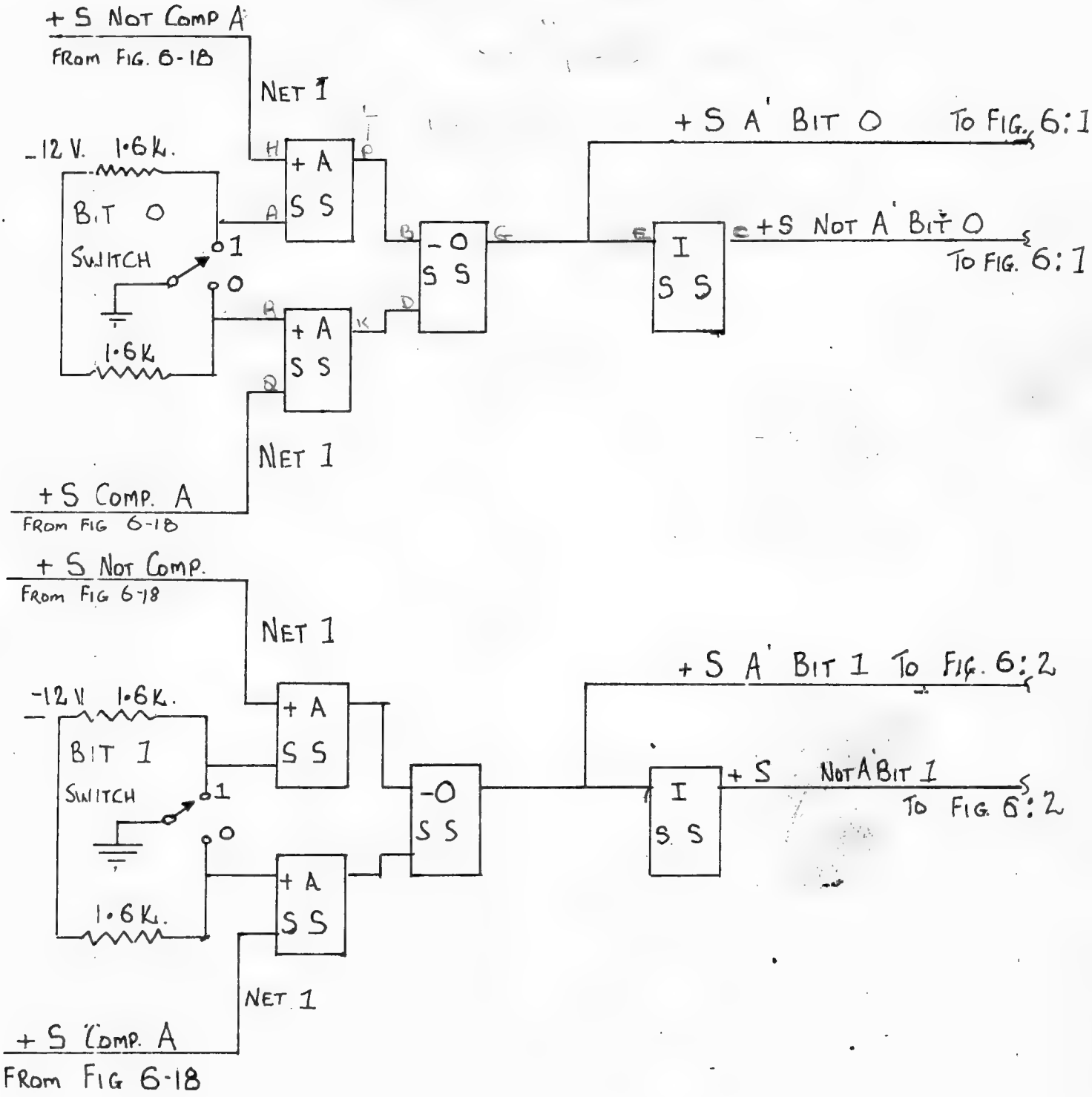


FACTOR ASSEMBLER

A

BITS 0 & 1

Fig: 6 - 9

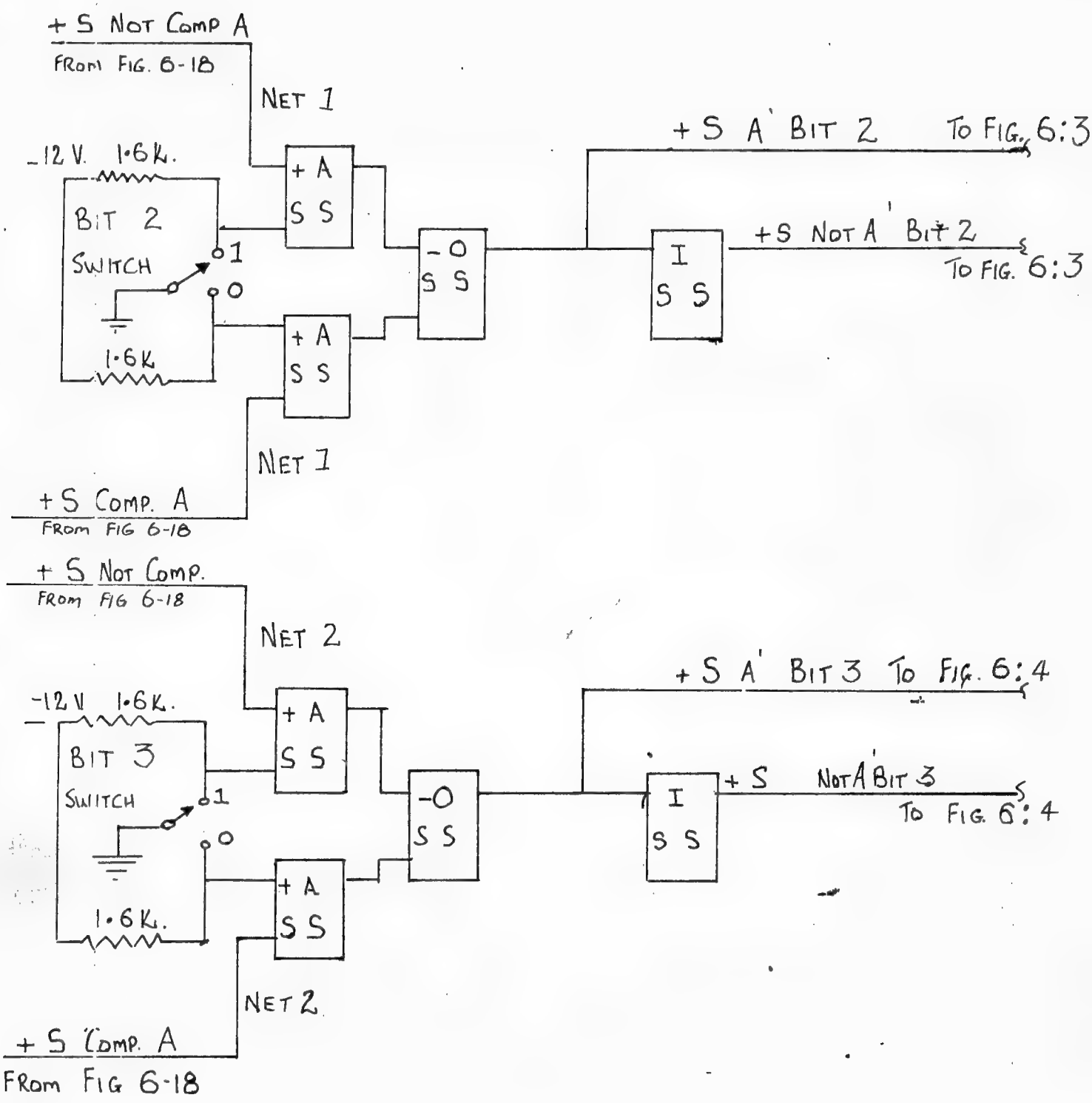


FACTOR ASSEMBLER

A

BITS 0 & 1

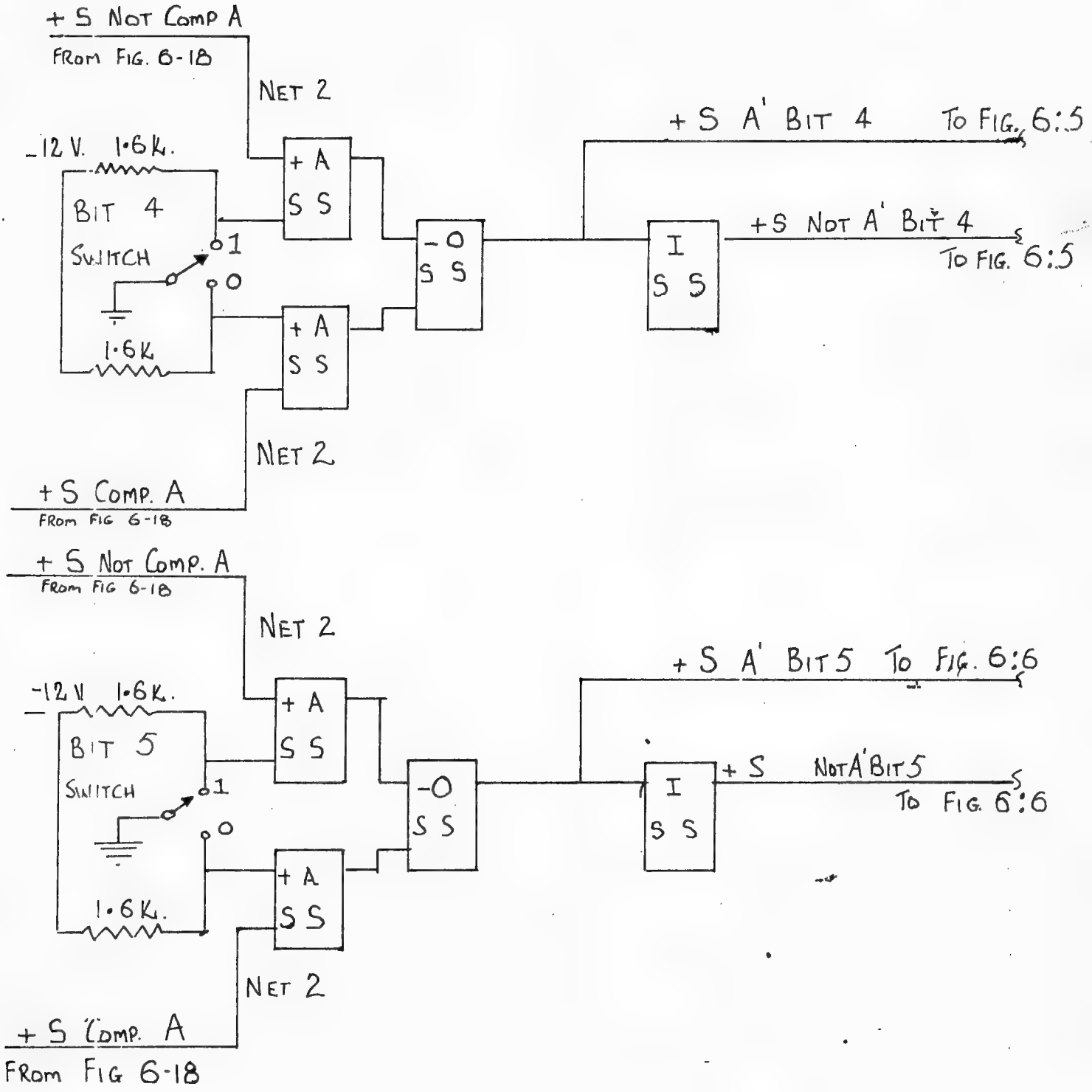
Fig:6 - 9



FACTOR A ASSEMBLER

BITS 2 & 3

Fig: 6 - 10

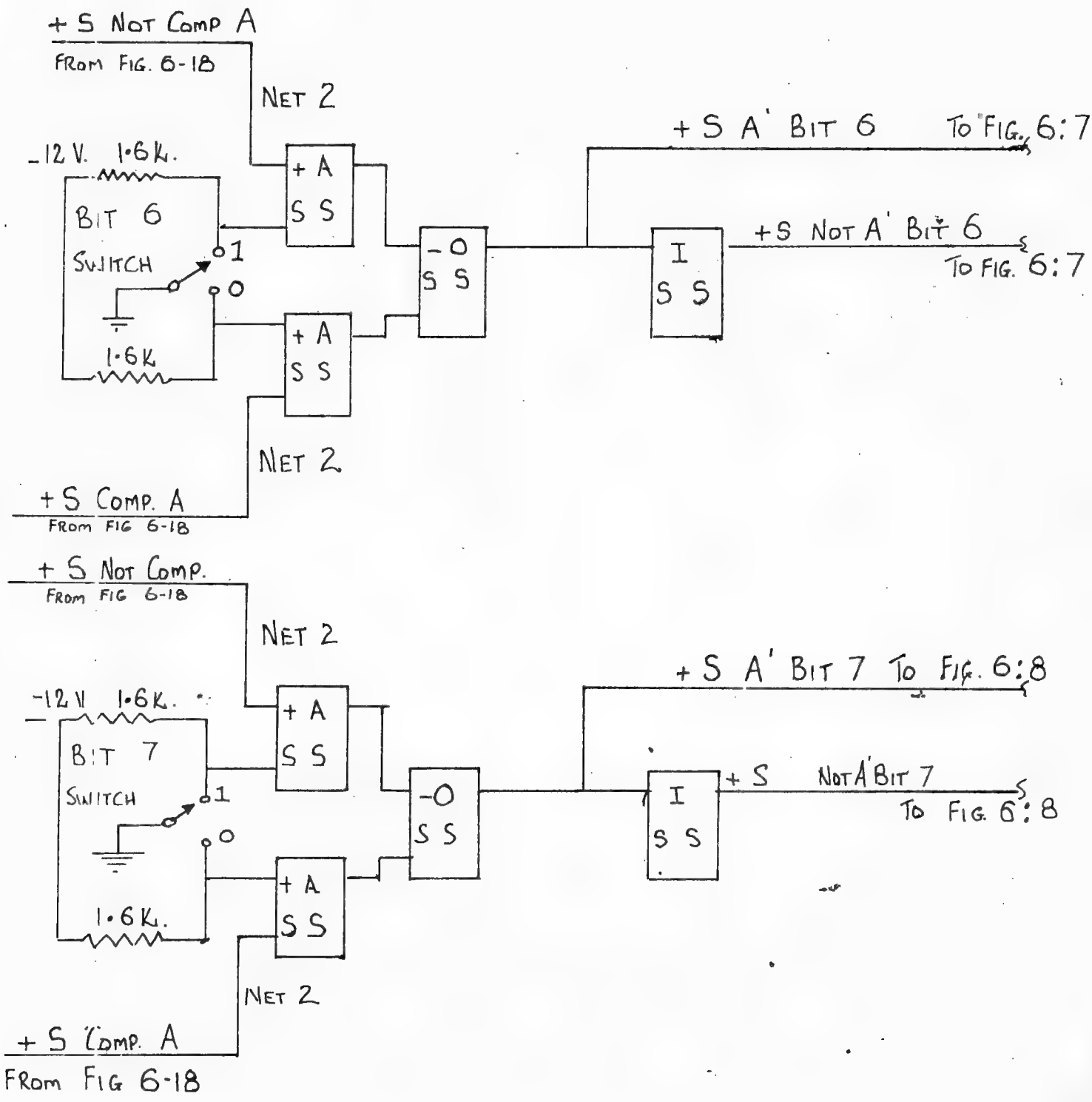


FACTOR ASSEMBLER

A

BITS 4 & 5

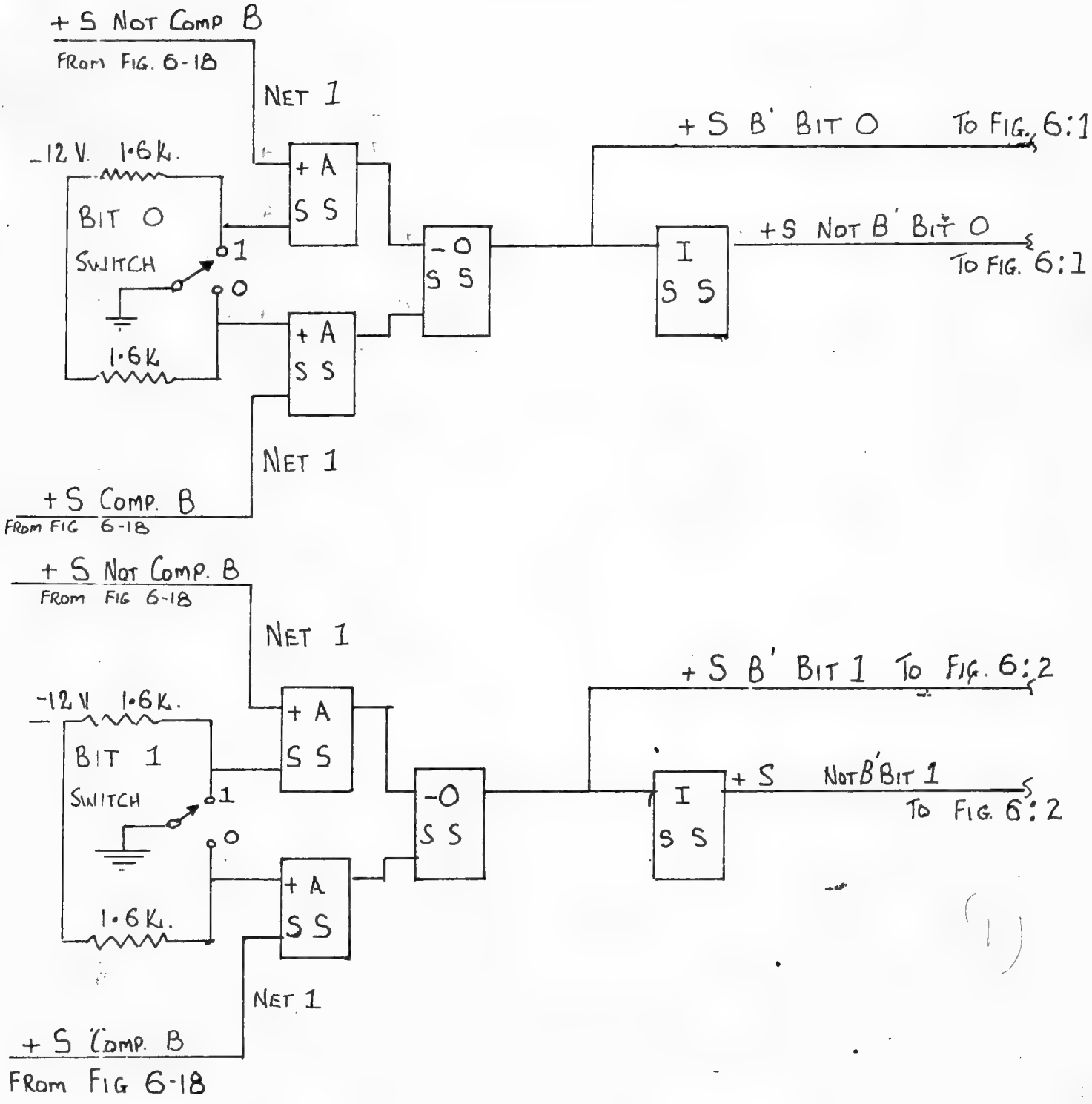
Fig: 6 - 11



FACTOR A ASSEMBLER

BITS 6 & 7

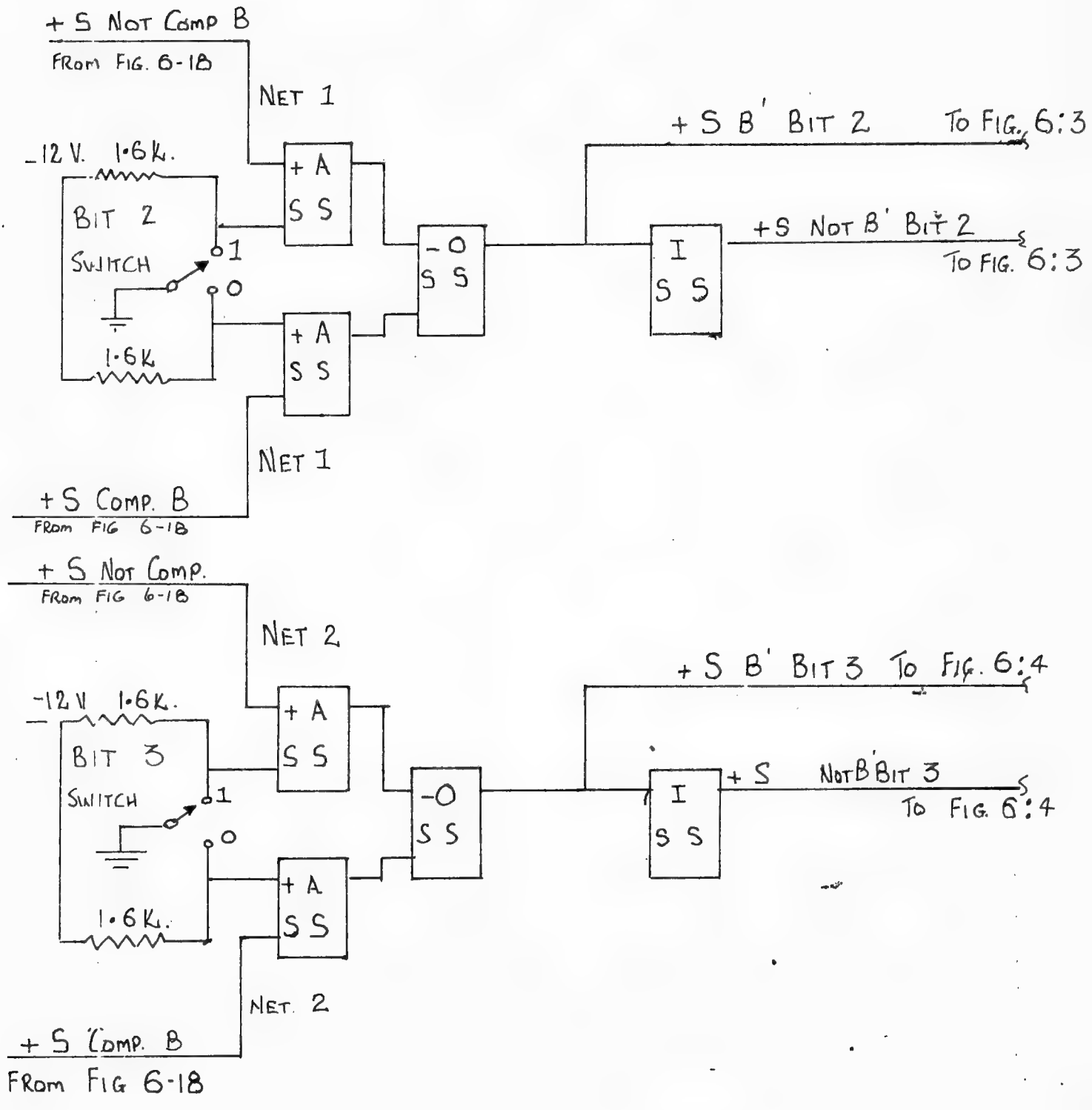
Fig: 6 - 12



FACTOR B ASSEMBLER

BITS 0 & 1

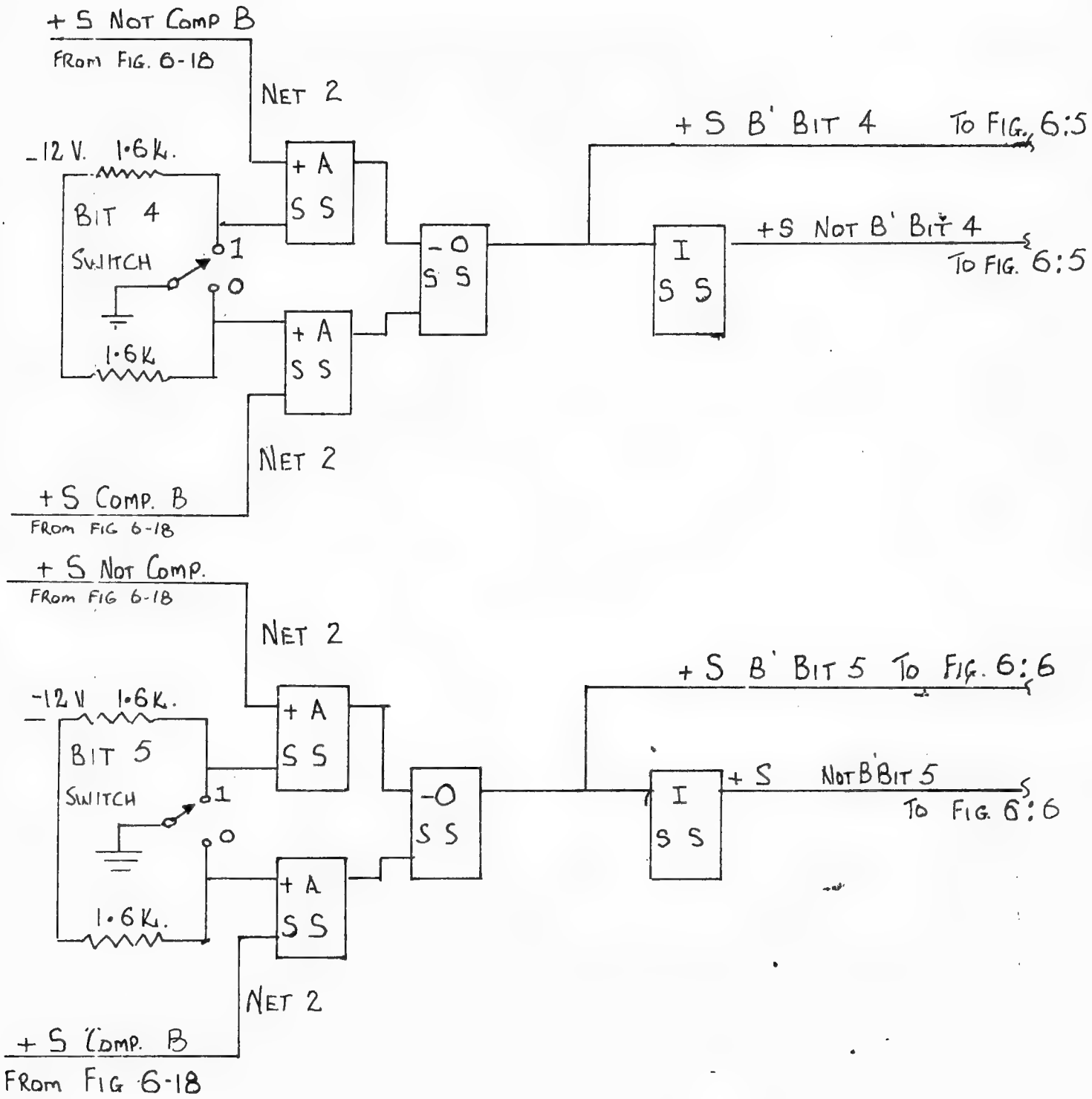
Fig: 6 - 13



FACTOR B ASSEMBLER

BITS 2 & 3

Fig: 6 - 14

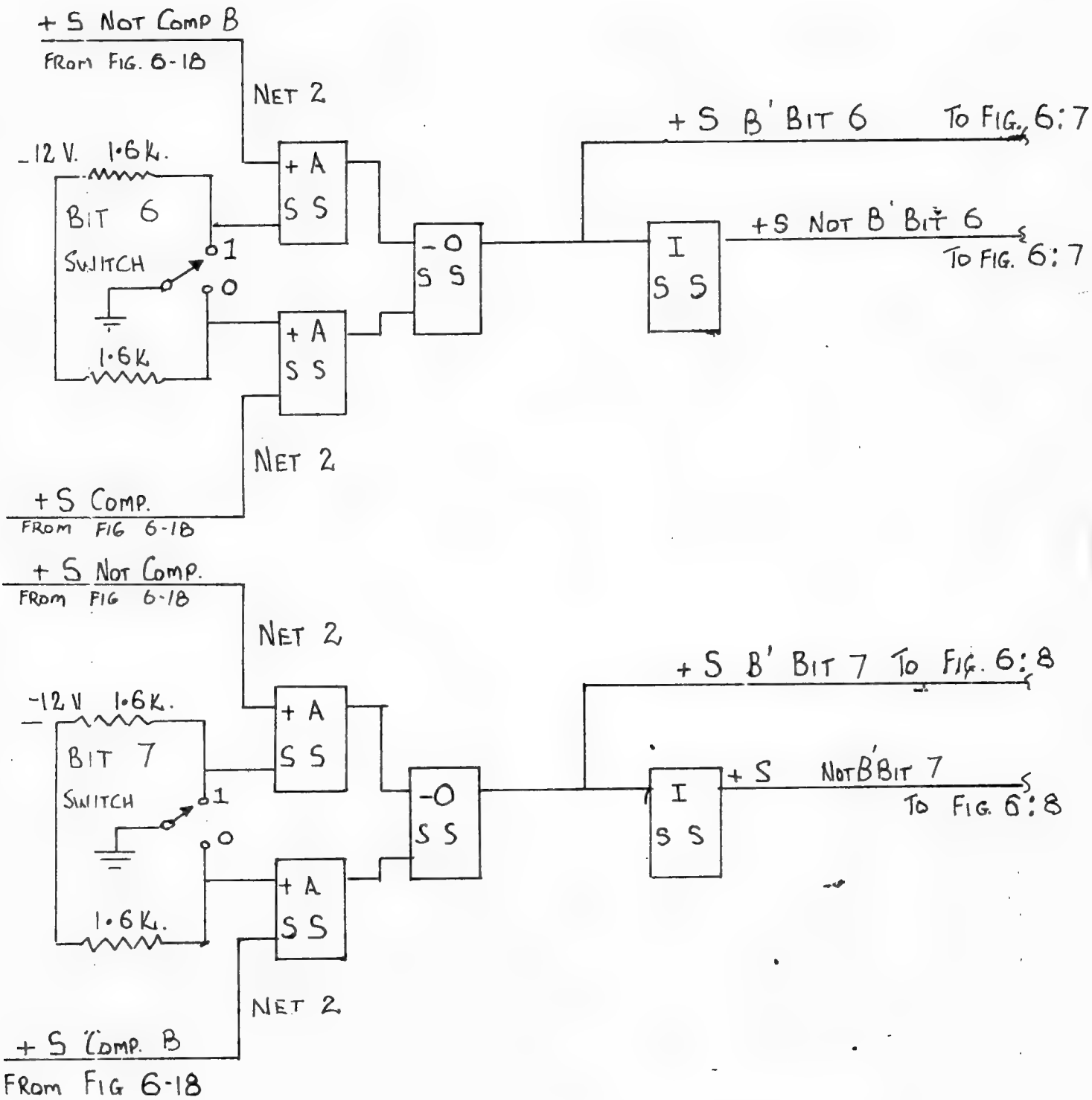


FACTOR ASSEMBLER (5

B

BITS 4 & 5

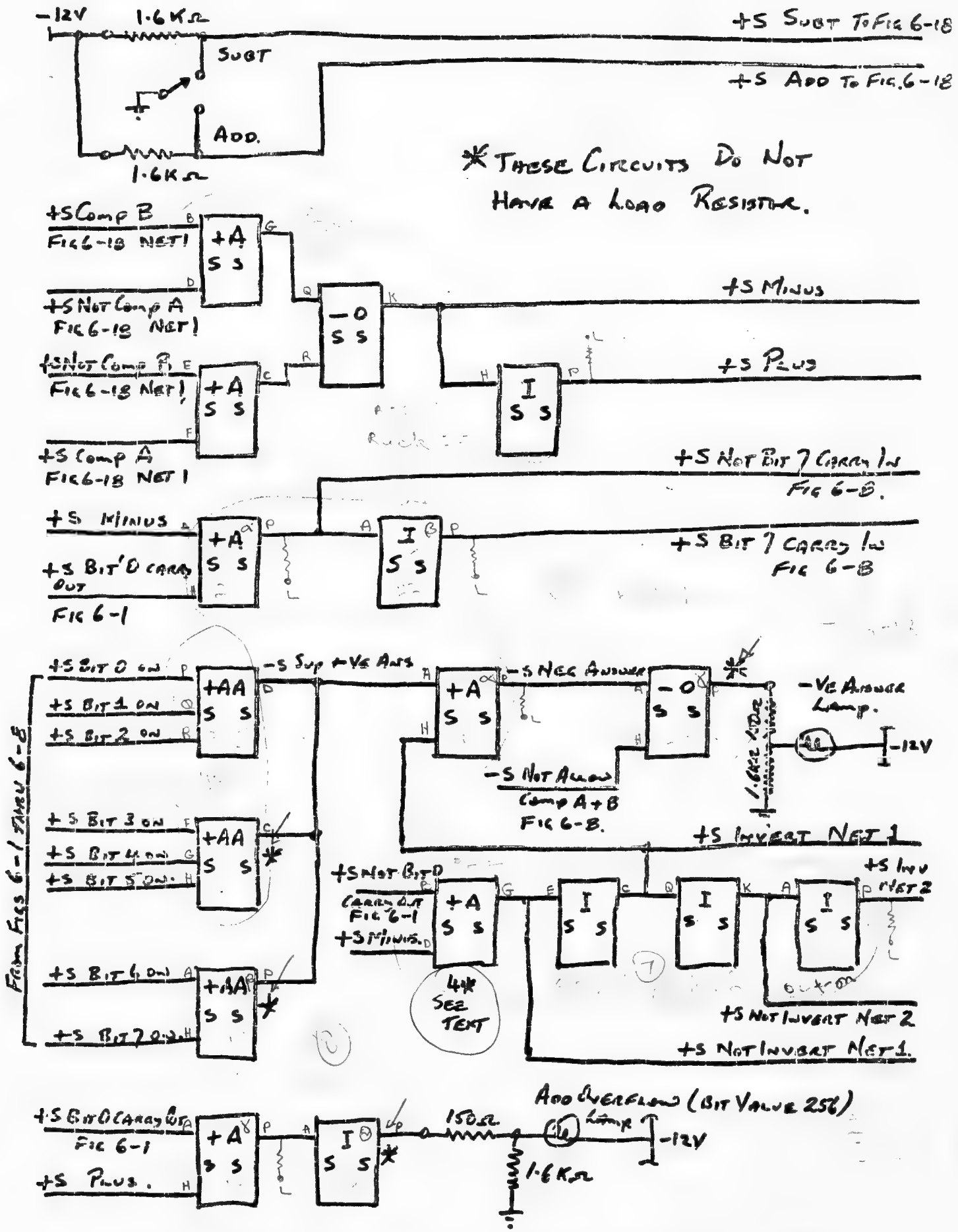
Fig: 6-15



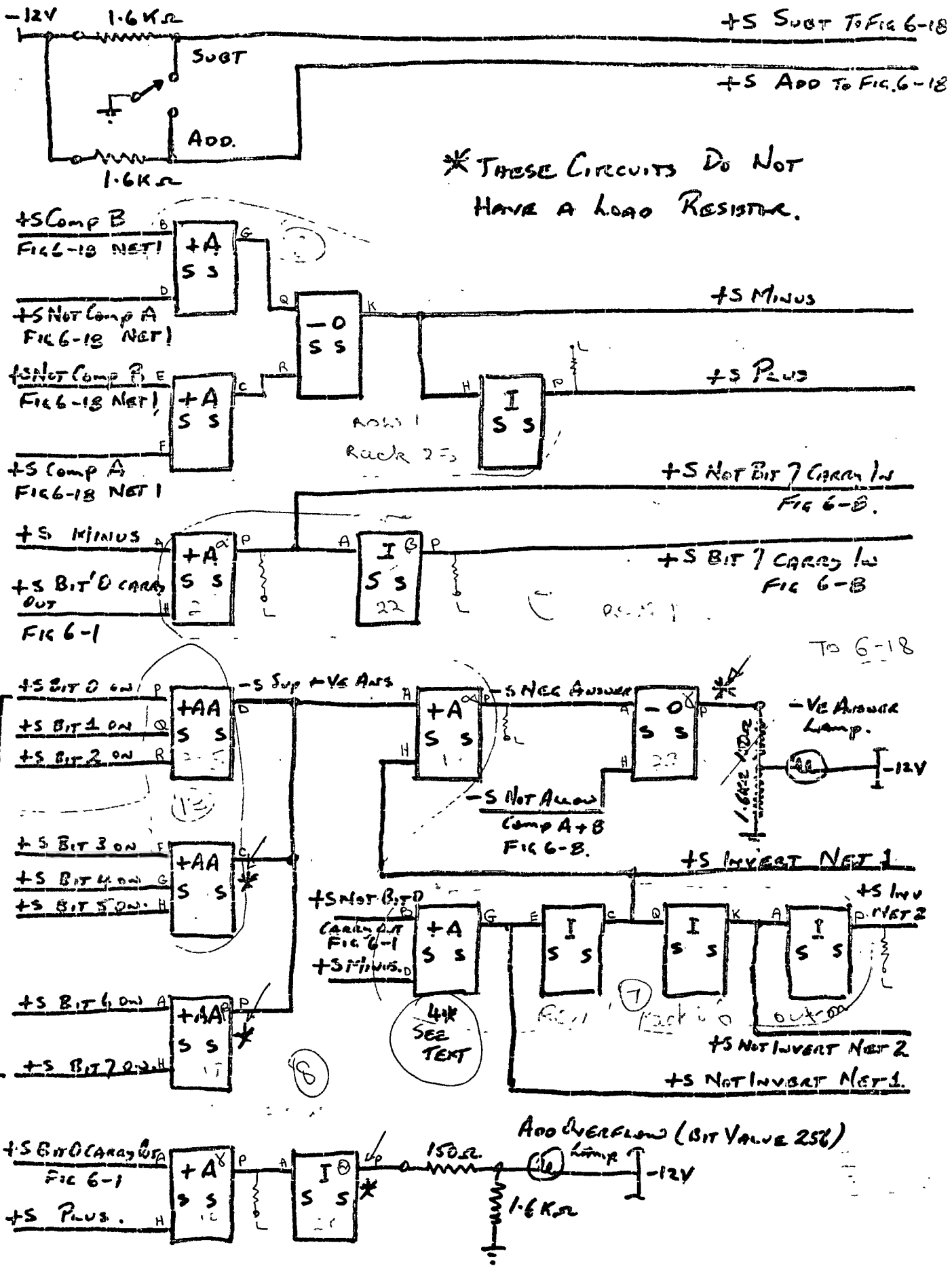
FACTOR B ASSEMBLER

BITS 6 & 7

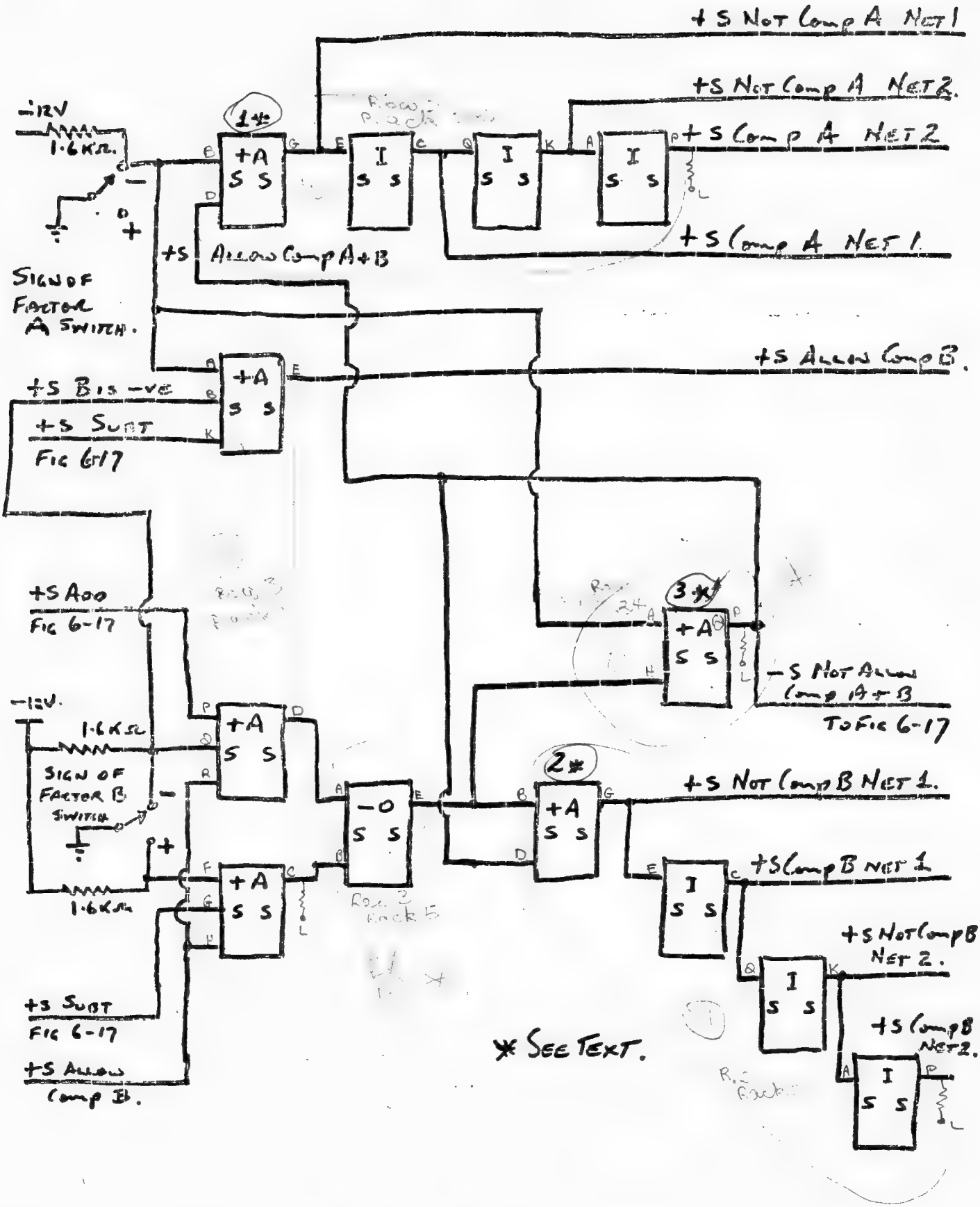
Fig: 6 - 16



ADD/SUBT — INVERT AND MISC CONTROLS. FIG. 6-17.

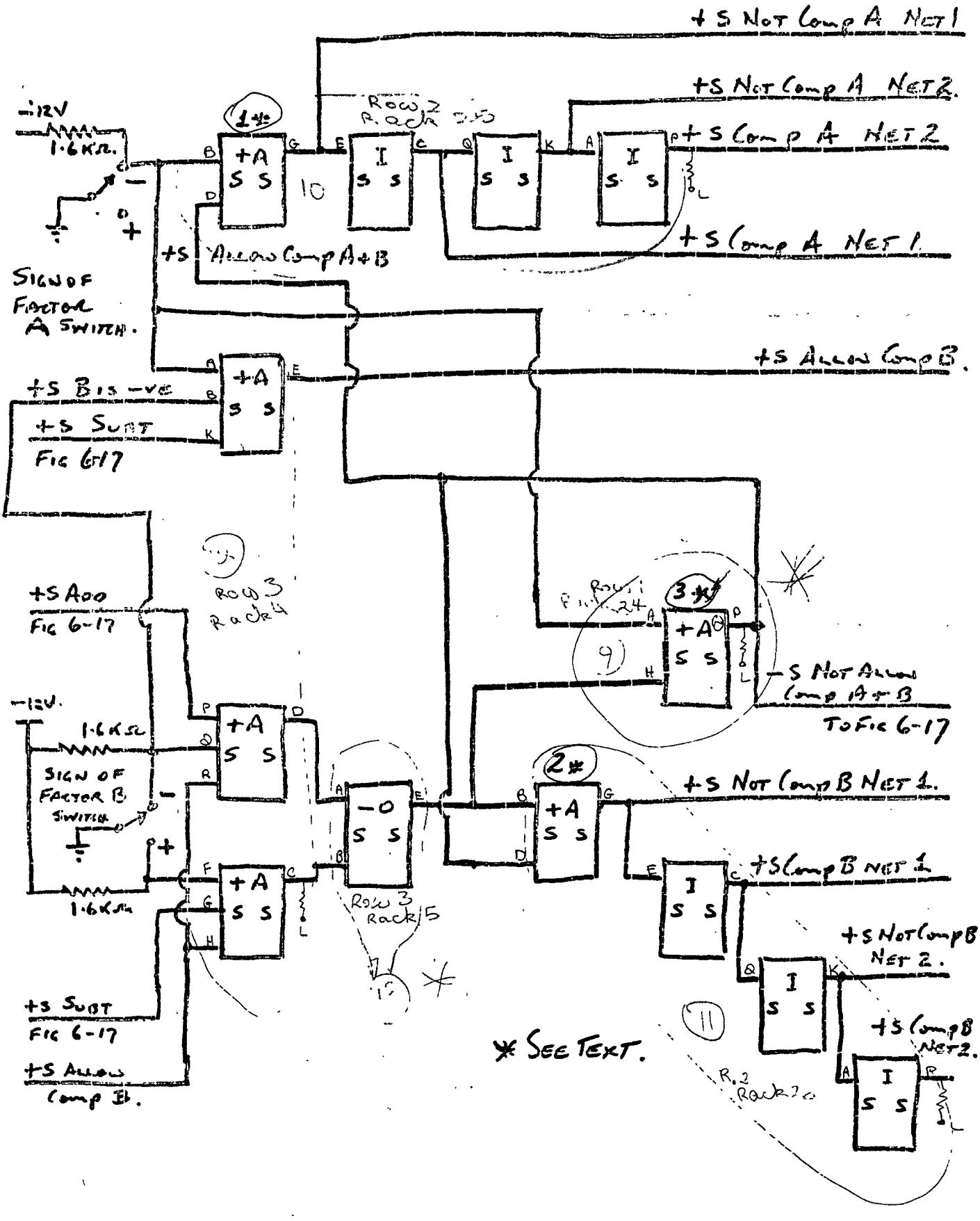


ADD/SUBT — INVERT AND MISC CONTROLS. FIG. 6-17.



Factor A and B Assembler Controls.

Fig 6-18.



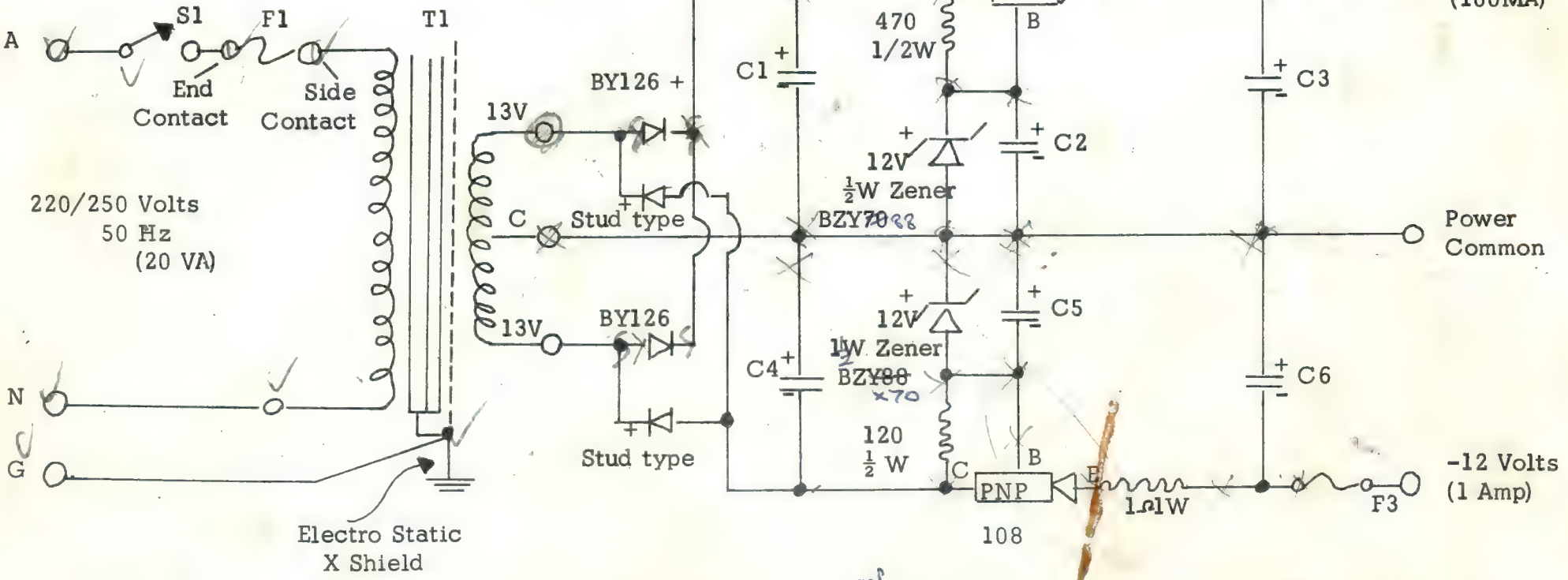
Factor A and B Assembler Controls.

Fig 6-18.

SIGNED ASSYNCHRONOUS BINARY ADDER

CHAPTER 7

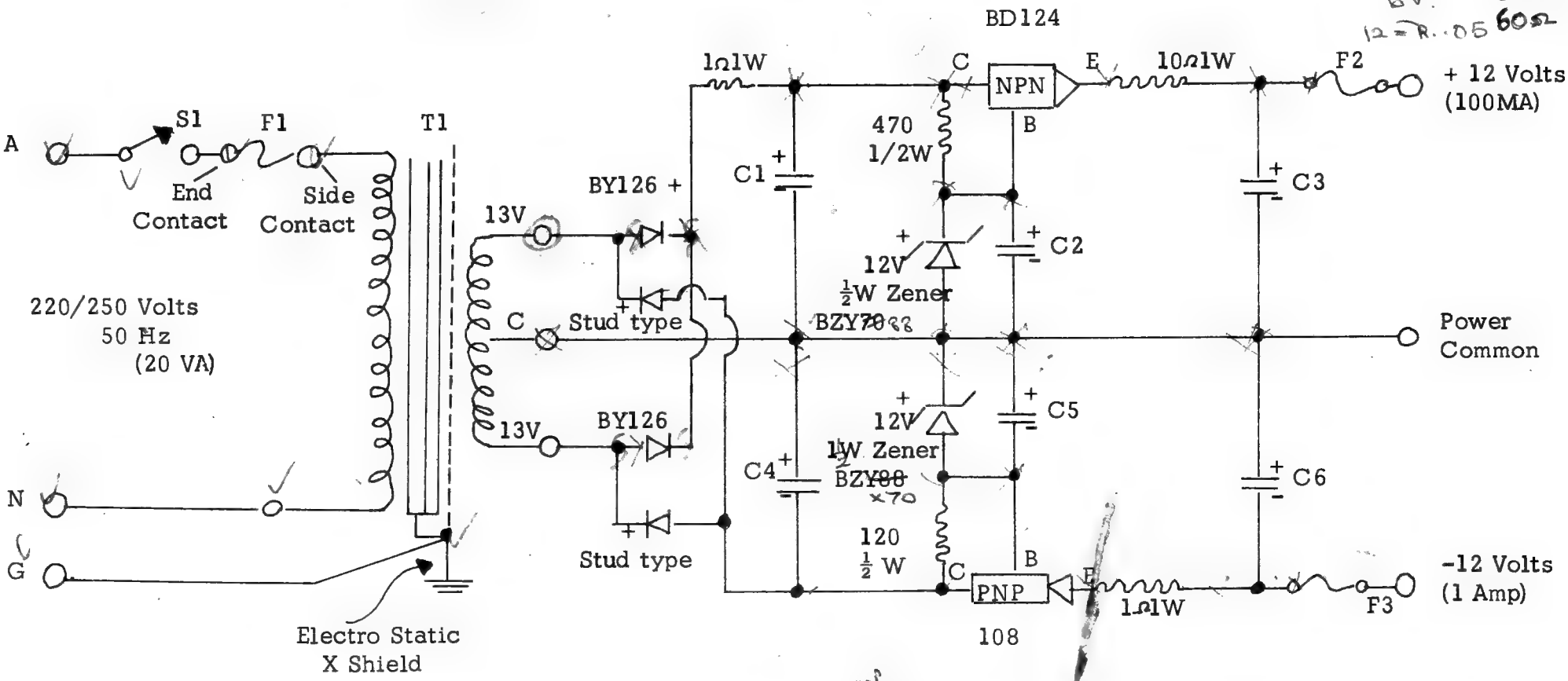
POWER SUPPLY AND CONSTRUCTION.



SUGGESTED POWER SUPPLY
SABA

C1 - C4	5000 ~~wt~~ 20VW	F1	.25Amp Blow
C2 - C5	1000 ~~wt~~ 16VW	F2	.25Amp Fast
C3	1000 ~~wt~~ 16VW	F3	2Amp Fast
C6	5000 ~~wt~~ 12VW		

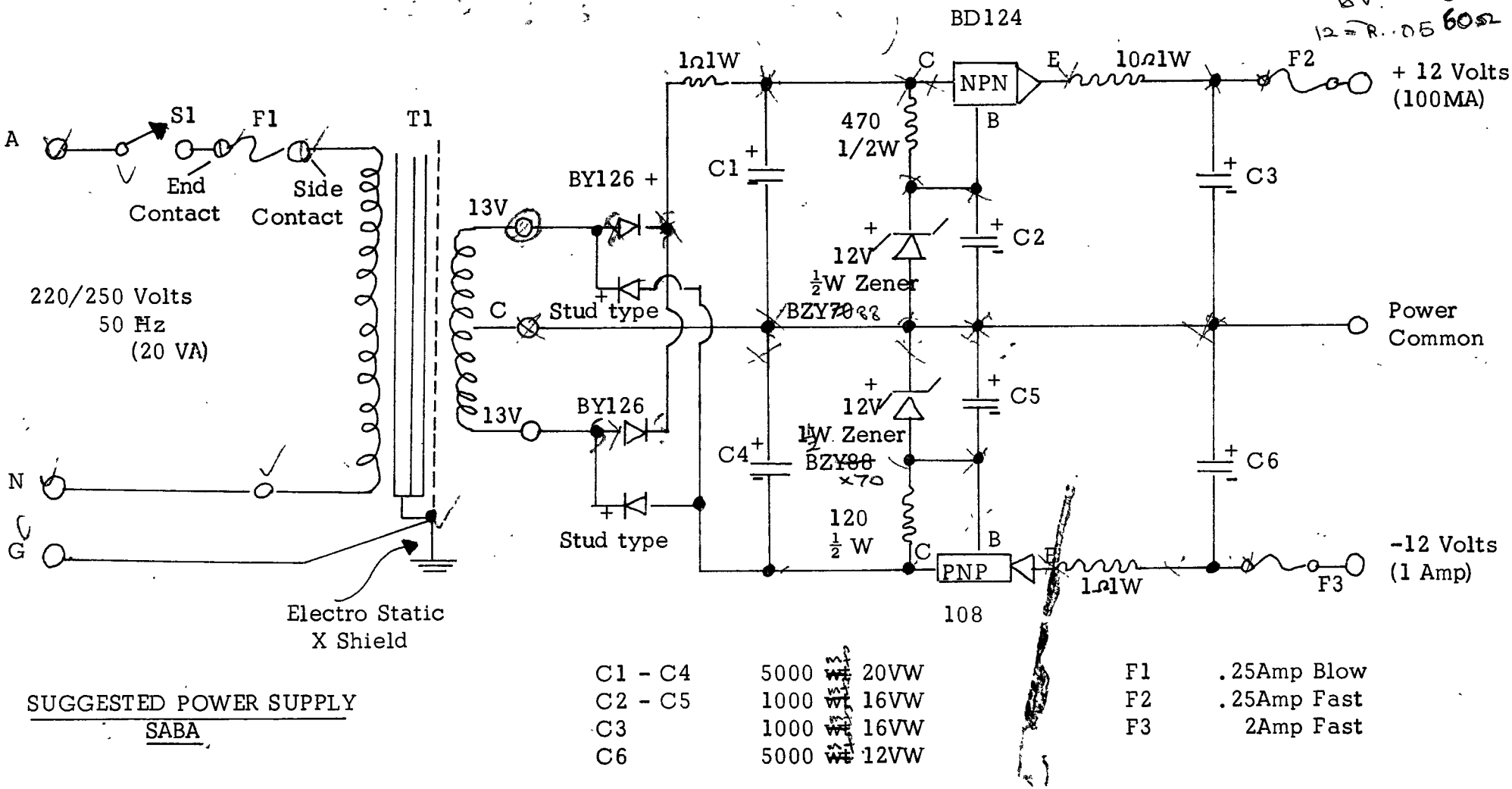
NOTE - Any larger value capacitors may be used as long as the working voltage is at least as high as shown



SUGGESTED POWER SUPPLY
SABA

C1 - C4	5000 ~~mf~~ 20VW	F1	.25Amp Blow
C2 - C5	1000 ~~mf~~ 16VW	F2	.25Amp Fast
C3	1000 ~~mf~~ 16VW	F3	2Amp Fast
C6	5000 ~~mf~~ 12VW		

NOTE - Any larger value capacitors may be used as long as the working voltage is at least as high as shown



C1 - C4	5000 µf 20VW	F1	.25Amp Blow
C2 - C5	1000 µf 16VW	F2	.25Amp Fast
C3	1000 µf 16VW	F3	2Amp Fast
C6	5000 µf 12VW		

NOTE - Any larger value capacitors may be used as long as the working voltage is at least as high as shown

SUGGESTED POWER SUPPLY
SABA

SIGNED ASSYNCHRONOUS BINARY ADDER

CHAPTER 8

SMS WIRE WRAPPING

CHAPTER 8

SMS WIRE WRAPPING

Two levels of wrapped connections may be used. The first level is the wrap closest to the base of the pin. The second level is closest to the end of the pin. When making wraps in the field, the six turns must be adhered to or it may not be possible to get two satisfactory wraps on one pin.

1. Skin the wire to desired length. Wire stripper (P/N 462075) should be used. Any slight nick in the wire will cause the wire to break. The length of the skinned wire determines the number of turns of wire on the terminal. For example, when using 24-gauge wire, about 1/4" bare wire is required for each turn. Because six turns are required for an acceptable connection, the skinned length should be 1.1/2" (Figure 8.1A).

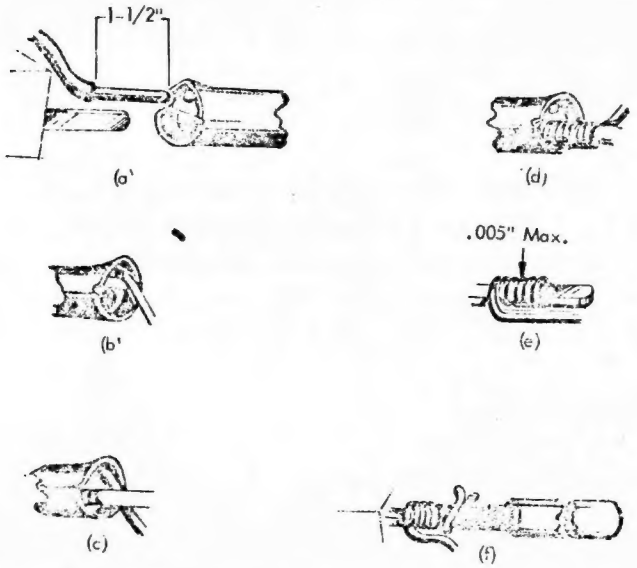


Figure 8.1 Wrapped-Wire Procedure

2. Insert the skinned wire into the small hole of the wrapping bit (Figure 8.1B) taking care to insert the wire up to the insulation. Do not bend the skinned portion of the wire; it may be difficult to slide into the bit.

SMS Wire Wrapping (continued)

2. continued

WARNING: If the wire is not inserted in the wrapping bit up to the insulation, a shiner (bare wire between insulation and terminal) may result. There should be one full turn of insulation at the beginning of each wrap.

3. Hold the wire with the fingers and bend the insulated portion of the lead into the retaining notch in the sleeve (Figure 8.1C). Use the right or left notch as determined by the direction of the approach (or exit) of the lead. Place the wrapping bit on the terminal. Be sure the terminal is inserted into the bit as far as it will go. Use reasonable care to hold the tool in line with the terminal.

4. Hold the tool on the terminal and rotate it clockwise to wrap the wire on the terminal. The tool will automatically recede as the wire coils on the terminal. The complete wrapped wire connection is shown in Figure 8.1D.

NOTE -

If too much pressure is used to push the tool on the terminal, a turn of wire may wrap over a previous turn. If too little pressure is exerted, the adjacent wraps of wire may not touch each other. Maximum separation between individual turns on the terminal must not exceed .005" excluding the first and last wrap (Figure 8.1E.

REMOVAL

Wires may be removed from a terminal by using wrap-unwrap tool, P/N 451142 (Figure 8.1F). The open end of the tool is placed over the terminal and rotated to the left, screwing the tool under the wraps of wire.

WARNING -

Once a wire is removed from a terminal, it may not be rewrapped. A new wire must be used or a new section of wire must be spliced to the existing wire.

SCHOOLS COMPUTER PROJECT PARTS LIST

	Qty	
SMS Card MX TAU AKV AHK CD	54 6	
Wire Wrap Tool	1	
Wire 24 G	As Required	
SMS Panel	11	
Lamp 10V 14mA	10	
Lamp Block 5 x 5	1	
Switch SPDT Power On/Off	1	
Switch Slide	20	
Resistor 150 ohm 1/2 watt	10	
Resistor 1.5Kohm 1/2 watt	45	
Resistor 120 ohm 1/2 watt	1	
Resistor 470 ohm 1/2 watt	1	
Resistor 10 ohm 1 watt	1	
Resistor 1 ohm 1.5 watt	2	
Capacitor 5000 uF20V	3	I
Capacitor 1000 uF 16V	3	
Diode Large for - 12V	2	II
Diode by 126/100 for + 12V	2	
Diode Zenner 12V . BZX70/C12	1	
Diode Zenner 12V . BZY88/C12	1	
Transistor 108 & Heat Sink	1	
Transistor BD 124	1	
Fuse Holder	3	
Fuse .25 amp Slow	1	
Fuse .25 amp Fast	1	
Fuse 2.0 amp Fast	1	
Power Transformer	1	
Power Cord	1	

NOTES -

I Or larger cap or higher voltage

II Any stud mounting Diode

Minor variations may occur in the parts supplied but these will be shown on the packing list with actual parts.